Department of Electronics & Telecommunication Engg.

LAB MANUAL

SUBJECT:-DIGITAL COMMUNICATION SYSTEM
[BTEC-501]

B.Tech– V Semester [2013-14]
(Branch: ETE)

KCT COLLEGE OF ENGG & TECH.,
FATEHGARH

PUNJAB TECHNICAL UNIVERSITY

TABLE OF CONTENTS

EXPERIMENT NO. :- 01

Aim: Study of Time Division Multiplexing System.

Apparatus Used: 1. TDM PCM Modulation Transmitter Trainer
2. C.R.O
3. Connecting leads

Theory:

Time Division is a technique of transmitting more than one information on the same channel. The samples consists of short pulses followed by another pulse after a long time intervals, this is as shown in fig.1

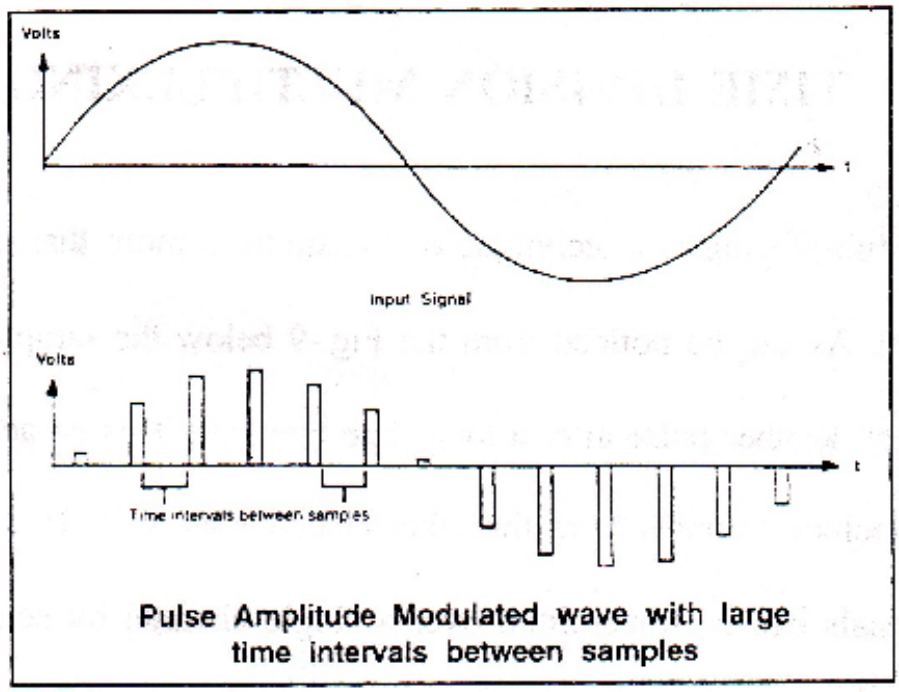


Fig.1

This no-activity time intervals can be used to include samples from the other channels as well. This means that several information can be transmitted over a single channel by sending samples from different information sources at different moments in time. This technique is known as Time Division Multiplexing or TDM. TDM is widely used in digital communication systems to increase the efficiency of the transmitting medium. TDM can be

achieved by electronically switching the samples such that they interleave sequentially at correct instant in time without mutual interference.

Procedure:

1. First set up the following initial conditions:
    a) Mode switch in FAST position.
    b) DC1 & DC2 controls in Function Generator Block fully clockwise.
    c) 1 KHz and 2 KHz signal control levels set to give 10 Vpp.
    d) Error check code generator switch A & B in A=0 & B=0 position
    e) All switched faults off.
2. Now connect only the 1 KHz output to Ch 0. Turn ON the power and check that the PAM output of 1 KHz sine wave is available at t.p.15 of the kit.
3. Connect channel I of CRO to tp. 10 and channel II of CRO to tp.15. Now observe the timing & phase relation between the sampling signal and the sampled waveform.
4. Now also connect 2 KHz supply to CH1. Connect channel 1 of the CRO to tp.12 and channel II of CRO to tp.15.
5. Observe the waveforms and relate the timing signals.

Observation:

Result: Time Division Multiplexing System has been studied.

Precautions:

1. Check the connections before switching On the kit.
2. Connections should be done properly.
3. Observation should be taken properly.

EXPERIMENT No. : 02

Aim: To study Pulse Code Modulation and Demodulation technique.

Apparatus Used: 1. PCM modulation / demodulation ST2103 trainer.
2. C.R.O
3. Connecting leads

Theory:

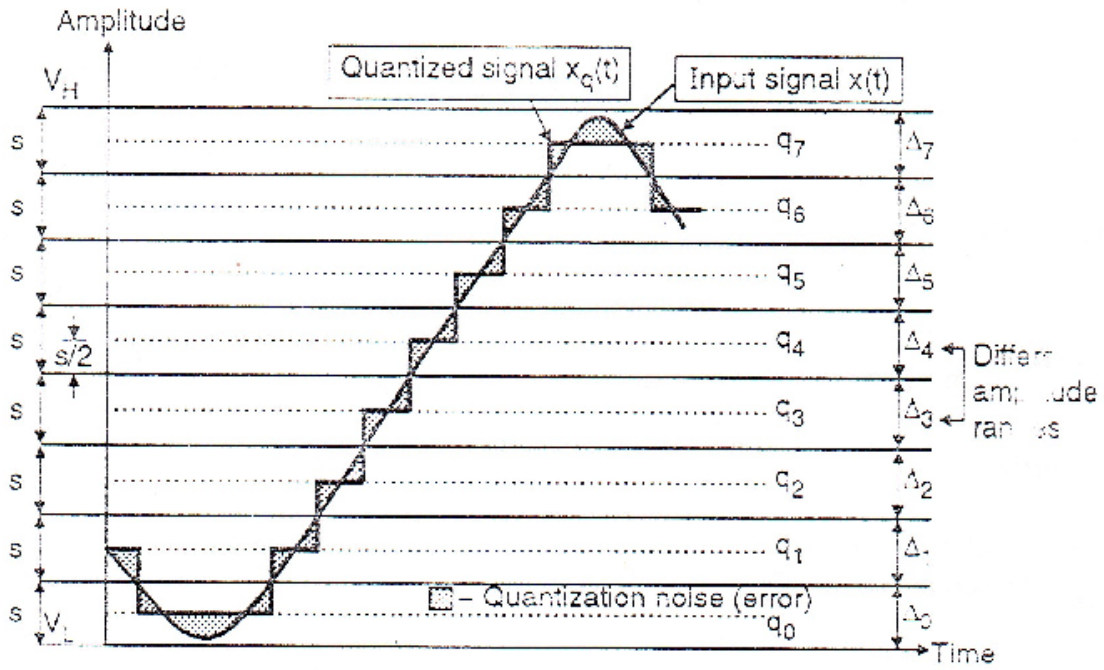
Pulse Code Modulation technique involves following steps:

(a) Sampling:

The analog signal is sampled according to the nyquist criteria. The nyquist criteria states that for faithful reproduction of a band limited signal, the sampling rate must be at least twice the highest frequency component present in the signal. So sampling frequency ≥ 2 fm, where fm is maximum frequency component present in the signal. Practically the sampling frequency is kept slightly more than the required rate.

(b) Allocation of binary codes:

Each binary word defines a particular narrow range of amplitude level. The sampled value is then approximated to the nearest amplitude level. The sample is then assigned a code corresponding to the amplitude level, which is then transmitted.This process is called quantization and it is generally carried out by the A/D Converter as shown below in fig1.



Process of quantization

Fig.1

Procedure:

1. Ensure that the MODE switch should be in FAST mode.
2. Connect CH 0 & CH 1 to DC1 AND DC2.
3. Ensure that the DC1 and DC2 controls in Function Generator Block should be in fully clockwise direction and ~1KHz and 2 KHz signal controls set art 10Vpp.
4. Now turn ON the kit and see that the LED glows.
5. With the help of Digital Voltmeter, adjust the DC1 amplitude control until the DC1 output measures 0V.
6. Observe the output on the A/D Converter Block LED's (D0 to D6). The LED's represent the state of the binary PCM word allocated to the PAM sample being processed.
7. Adjust the D.C input from +5V to –5V in steps of 1V.
8. Observe the output of +5V is as follows:

D6	D5	D4	D3	D2	D1	D0
1	1	1	1	1	1	1

Where for the negative values it is less than 1000000.For –5V the output is as follows:

D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0

This is obtained at the approximately full anti clockwise position of the DC Control.

9. Turn the DC1 control fully anticlockwise and repeat the above procedure by varying the DC2 control.
10. Trigger the dual trace oscilloscope externally by the CH.1 signal available at t.p.12 and observe the signal at CH.0 and CH.1 at t.p.5 with reference to the signal at t.p.7.
11. Now connect the oscilloscope channel 1 to CH1 sample at t.p.6 and sketch the three waveforms.

Observations:

Result: The PCM Modulation / Demodulation studied.

Precautions:

1. Connections should be checked before switching ON the kit.
2. Observations should be taken properly.

EXPERIMENT No. : 03

Aim: To study delta modulation & demodulation and observe the effect of slope overload.

Apparatus Used: 1. Delta modulation / demodulation trainer.
2. C.R.O
3. Connecting leads

Theory : Delta Modulation is a system of Digital Modulation scheme in which the difference between the sample value at sampling time K and sample value at the previous sampling time (k – 1) is encoded into just a single bit. One way in which delta modulator and demodulator is assembled is as shown in fig.1 and fig.2.

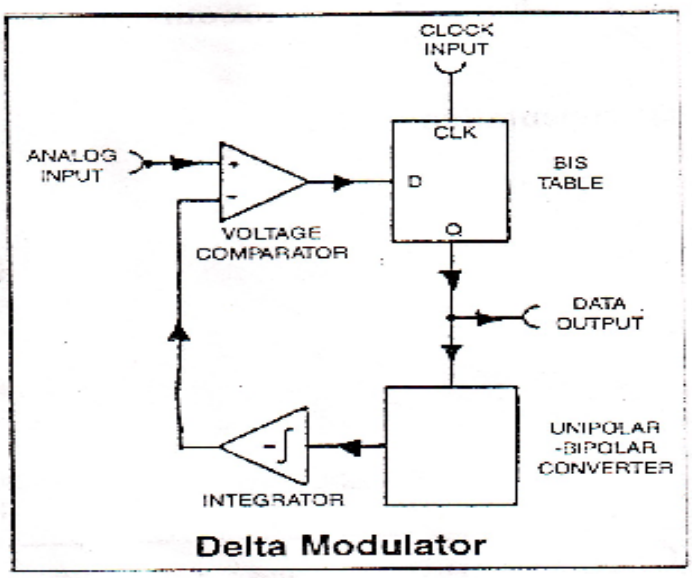


Fig.1

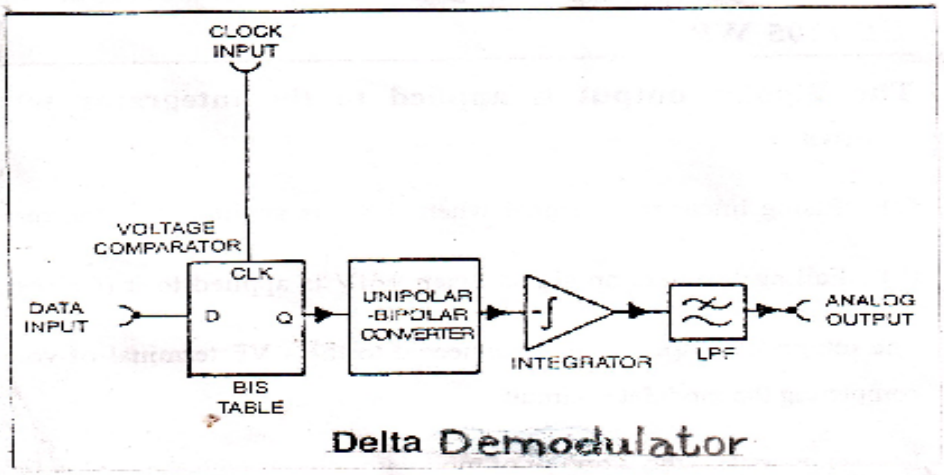


Fig.2

The baseband signal m(t) and its quantized approximation m'(t) are applied as inputs to a comparator. A comparator simply makes a comparison between inputs. If signal amplitude has increased, then modulators output is at logic level 1. If the signal amplitude has decreased, the modulator output is at logic level 0. Thus the output from the modulator is a series of 0's and 1's to indicate rise and fall of the waveform since the previous value. The comparator output is then latched into a D flip-flop which is clocked by the transmitter clock. Thus the output of the flip-flop is a latched 1 or 0 synchronous with the transmitter clock edge. The binary sequence is transmitted to receive and is also fed to the unipolar to bipolar converter. This block converts logic 0 to voltage level of +4V and 1 to voltage level of – 4V. The bipolar output ia applied to the integrator whose output is : a) Rising linear ramp signal when – 4V is applied to it

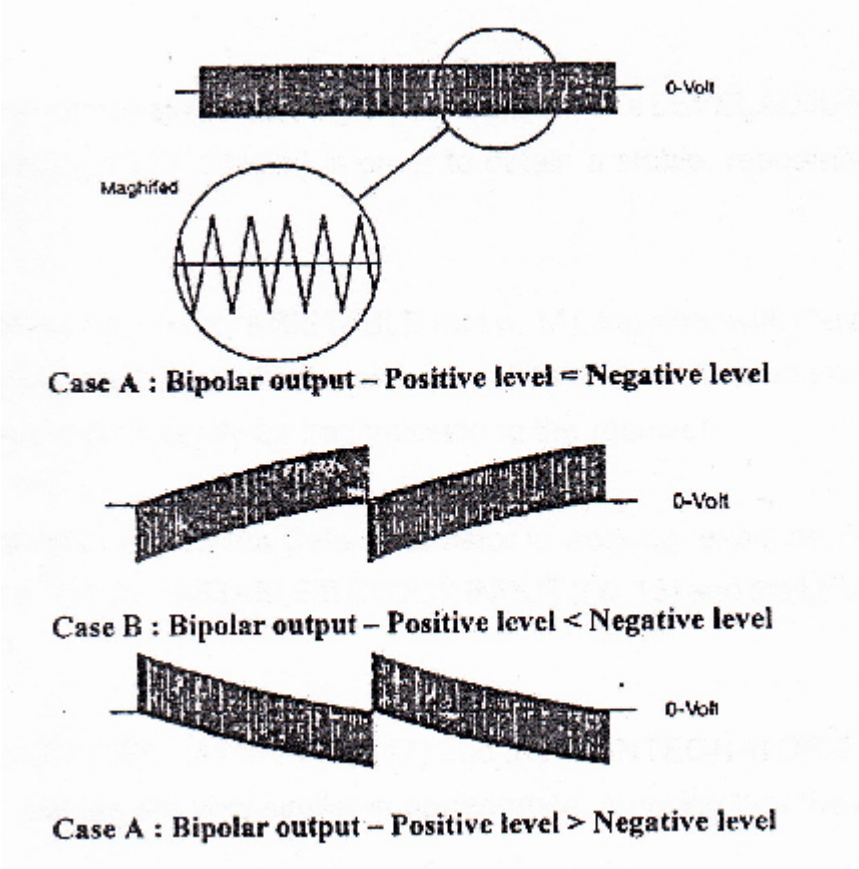
b) Falling linear ramp signal when + 4V is applied to it.

The integrator output is then connected to the – ve terminal of voltage comparator.

Procedure:

1. Make connections as per diagram.
2. Ensure that the clock frequency selector block switches A & B are in A=0 and B=0 position.
3. Now turn On the kit and see that LED glows.
4. In order to ensure for the correct operation of the system, we first connect 0 volts to the +ve input of the comparator. Now observe the output of the integrator 1 (i.e. tp 17) and the output of transmitter's level changer (i.e. tp 15). When the positive and negative output levels of the level changer will be equal the output will be a triangular waveform as shown in fig3 (Case A). When the negative level is greater than positive level, the integrator's output level will be as shown in fig3 (Case B). And when the positive output level is greater, then the integrator's output will be as shown in fig3 (Case C). The levels can be adjusted by turning the potentiometer from one extreme to another.
5. Adjust the transmitter's level changer preset until the output of integrator is a triangular wave centered at 0 volts. The peak to peak amplitude of the wave should be 0.5 volts (approx.), this amplitude is known as the integrator Step Size.
6. Now observe the output of the transmitter's bistable circuit (i.e. tp 14). It is now a stream of alternate '1' and '0'. This is the output of a delta modulator and the Delta modulator is now said to be balanced for correct operation.
7. Now examine the output of integrator at the receiver (i.e. tp 47). It should be a triangular wave with step size equal to that of integrator in transmitter and ideally centered around 0 volts.
8. Now observe the output of low pass filter. It will be a DC level centered around 0 volts. This is the output of Delta demodulator and it is balanced for correct operation.
9. Now disconnect the 0 volts from the +ve input of the comparator and reconnect it to 250 Hz signal of the function generator block. Now observe the output of voltage comparator (tp 9), integrator (tp 17). Also observe the delta modulated output at the output of bistable circuit. It has been encoded into stream of '0' and '1'.
10. Also observe the output of low pass filter in the receiver (tp 51), which is the output of demodulator.
11. Now disconnect 250 Hz from the +ve input of comparator and reconnect it to 500 Hz , 1 Khz, and 2 Khz outputs in turn. Now note the frequency of the analog signal increases, so the low pass filter's output becomes more distorted and reduced in amplitude. This effect is known as 'Slope Overloading'.

Observations:



Result: The Delta modulation / demodulation and Slope Overloading effect has been studied.

Precautions:

1. The connections should be made properly and tightly.
2. Check all the connections before switching ON the kit.

EXPERIMENT No. : 04

Aim : Study of Pulse data coding techniques.

Apparatus Used :

1. Data Encoding kit (Trainer 2106)
2. Data bit generator
3. Patch cords
4. CRO
5. CRO Probes

Block Diagram:

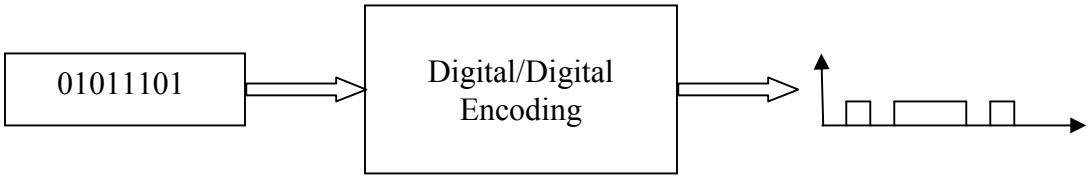
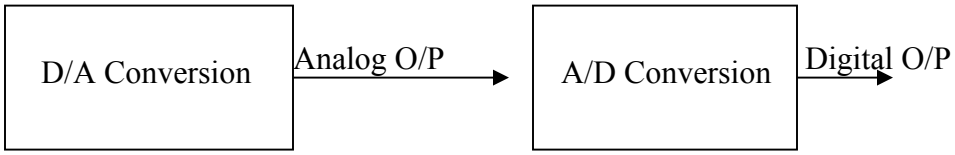


Fig 1: Digital-to-Digital Encoding



Theory: Digital to Digital conversion is the representation of digital information by a digital signal. In this conversion, the binary 1's and 0's generated by a computer are translated into a sequence of voltage pulses that can be propagated over a wire. Fig1 shows the relationship between the digital information, the digital-to-digital encoding hardware and the resultant digital signal. There are many mechanisms for digital-to-digital conversion; these are unipolar, polar and bipolar encoding/conversion. In our present experiment we are using polar conversion method.

Polar Encoding: It uses two-voltage levels- one positive and one negative. Of many existing variations of polar conversion we will examine only the three most popular: nonreturn to zero (NRZ), return to zero (RZ), and biphase. NRZ encoding includes two methods: nonreturn to zero, level (NRZ-L), and nonreturn to zero, invert (NRZ-I). Biphase also refers to two methods. The first, Manchester, is the method used by Ethernet LANs. The second, Differential Manchester, is the method used by Token Ring LANs.

Nonreturn to Zero(NRZ): In NRZ encoding, the level of the signal is always either positive or negative. The two most popular method of NRZ transmission are:
NRZ-L: In this encoding method, the level of the signal depends on the type of bit it represents. A positive voltage usually means the bit is a 0, and a negative voltage means the bit is a 1(or vice-versa); thus, the level of the signal is dependent upon the state of the bit.

NRZ-I: In this method, an inversion of the voltage level represents a 1 bit. It is the transition between a positive and negative volatage, not the voltages themselves, that represents a 1 bit. A 0 bit is represented by no change.

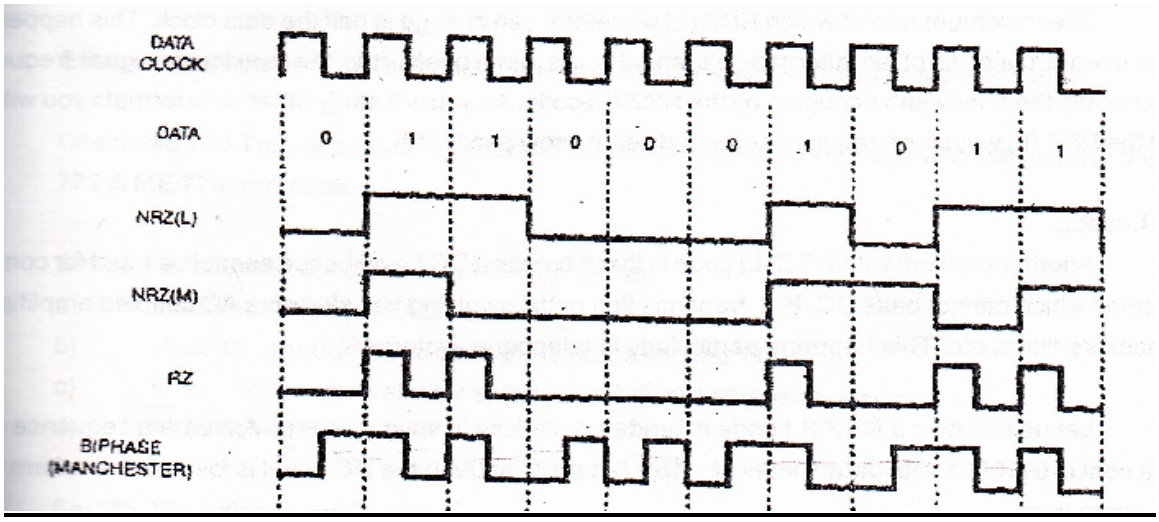
Return to Zero: This method uses three values: positive, negative and zero. The signal changes not between bits but during each bit. A positive voltage means 1 and negative voltage means 0.

Biphase: In this the signal changes at the middle of the bit interval but does not return to zero. Instead it continues to the opposite pole.

Procedure :

1. Data is generated with the help of a data bit generator.
2. Connect the data O/P of the data generator to the Tx data I/P of the trainer 2106.
3. Now connect the clock of the generator to the Tx clock of the kit and ground with the ground terminal of the kit.
4. Select the data on the data generator and load it in the trainer 2106 by pressing load button.
5. Now observe the O/P of the NRZ-L, NRZ-M and Biphase.

Observations :



Result :
Different pulse data coding techniques has been studied.

Precautions:

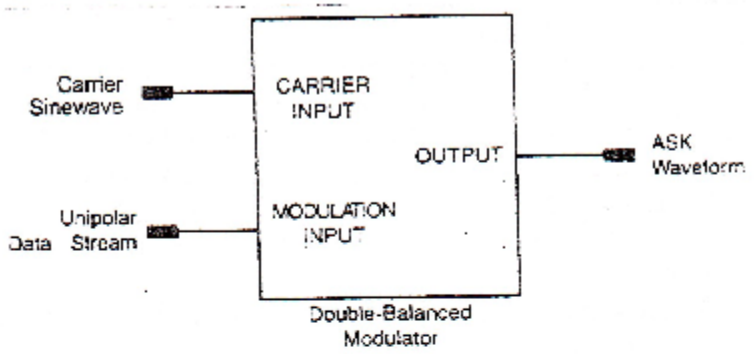
1. The connections should be made properly and tightly.
2. Check all the connections before switching ON the kit.

EXPERIMENT No. : 05 & 06

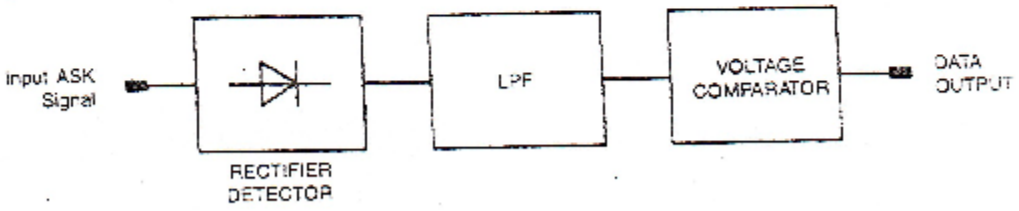
Aim:
1. Study of data decoding techniques for various formats.(exp. no. 5 as per syllabus).
2. Study of Amplitude Shift Keying Modulator and Demodulator.(exp. no. 6 as per syllabus).

Apparatus Used: ASK Modulator/Demodulator Trainer kit (ST 2106, ST 2107), Data Bit Generator, CRO, CRO Probes.

Block Diagram:



AMPLITUDE SHIFT KEYING Fig 1



ASK DEMODULATOR Fig 2

Theory: The simplest method of modulating a carrier with a carrier stream is to change the amplitude of carrier wave every time the data changes. This modulation technology is known as Amplitude Shift Keying.

ASK is obtained by switching ON the carrier to be obtained '1' and switching OFF when D=1, i.e. carrier is transmitted & D=0, i.e. carrier is suppressed. This technology is ON-OFF keying. Fig1 shows ASK for a given data stream. A linear multiplier generates it. O/P voltage is a product of ac coupled carrier and the information signal or modulating signal. For a

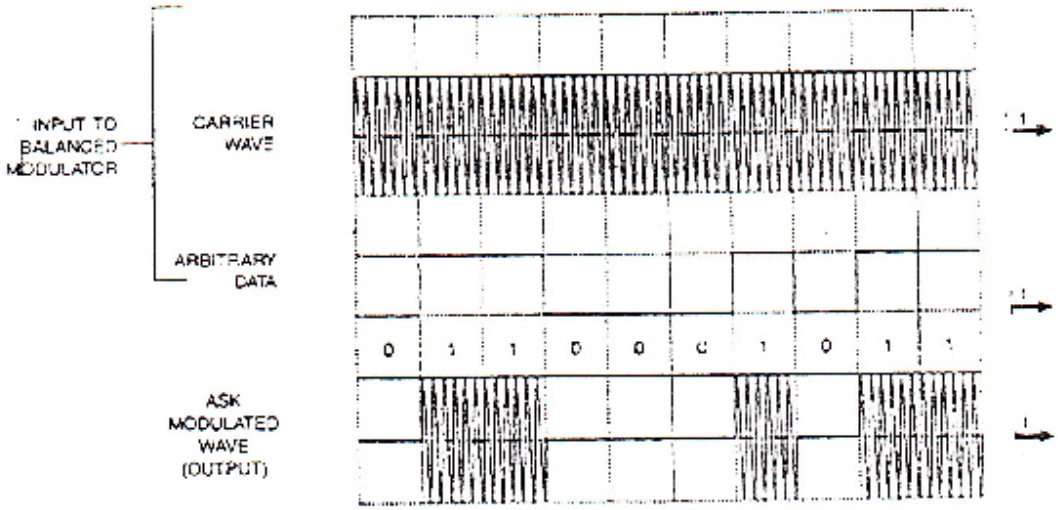
double balanced modulator, data stream applied is 0V at logic 0 & +5V at logic 1. The O/P is sine wave unchanged in phase when '1' is applied. Carrier is multiplied by +ve constant voltage when bit 0 is applied.

Fig 2. shows demodulator of ASK waveform at receiver. A diode rectifier first rectifies it. After rectification, signal is passed through Low Pass Filter to remove carrier. These rounded pulse are then squared up by passing it through voltage comparator set at a threshold level. If I/P volt > Threshold level; O/P is +5V.

Procedure:

1. Turn ON the trainer kits. Monitor NRZ(L) O/P (t.p.5) from ST2106 trainer on one channel of the CRO. Use the other channel to monitor the O/P of modulator 1 (t.p. 28) in ST2106 trainer.
2. Three variables have been provided in the modulator block. These may be necessary to obtain a required ASK waveform. These variables are:
   Gain: This potentiometer adjusts the amplification of the modulator's O/P. Adjust this pot till the O/P is not a 2 Vpp signal in 'ON' state.
   Modulation Offset: This control is used to adjust the amplitude of the OFF signal. Adjust this control till the amplitude of the off signal is as close to zero as possible.
   Carrier Offset: This control adjusts the off bias level of the ASK waveform. Adjust this control till the off level occurs midway between the ON signal peaks.
3. Observe the O/P at the ASK demodulator (t.p. 22) & LPF (t.p. 24) on ST2107) trainer.
4. Adjust the bias level till the O/P signal pulse width is not similar to the NRZ(L) data pulse width.

Observations:



ASK MODULATION

Result:

The ASK modulator and demodulator circuit has been studied.

Precautions:

1. Check the connections before switching ON the kit.
2. Observations should be taken properly.

EXPERIMENT No. : 07

Aim: Study of Frequency Shift Keying Modulator and Demodulator.

Apparatus Used: FSK Modulator/Demodulator Trainer kit (ST 2106, ST 2107), Binary Data Generator, CRO, CRO probes.

Block Diagram:

Block Diagram:

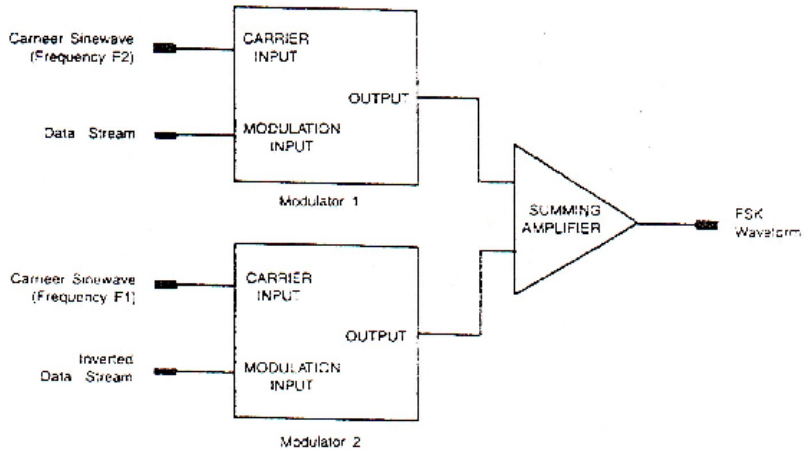


Fig 1 : FSK MODULATOR

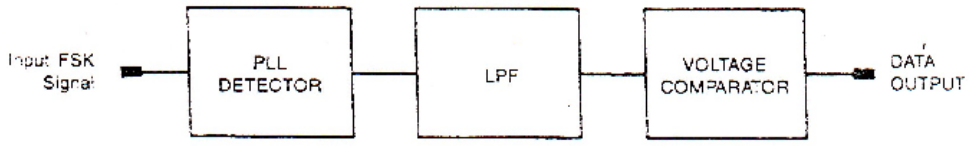


Fig 2 : FSK DEMODULATOR

Theory: In Frequency shift keying, the carrier frequency is shifted (i.e. from one frequency to another) corresponding to the digital modulating signal. If the higher frequency is used to represent a data '1' & lower frequency a data '0', the resulting FSK waveform appears. Thus

Data =1 High Frequency

Data =0 Low Frequency

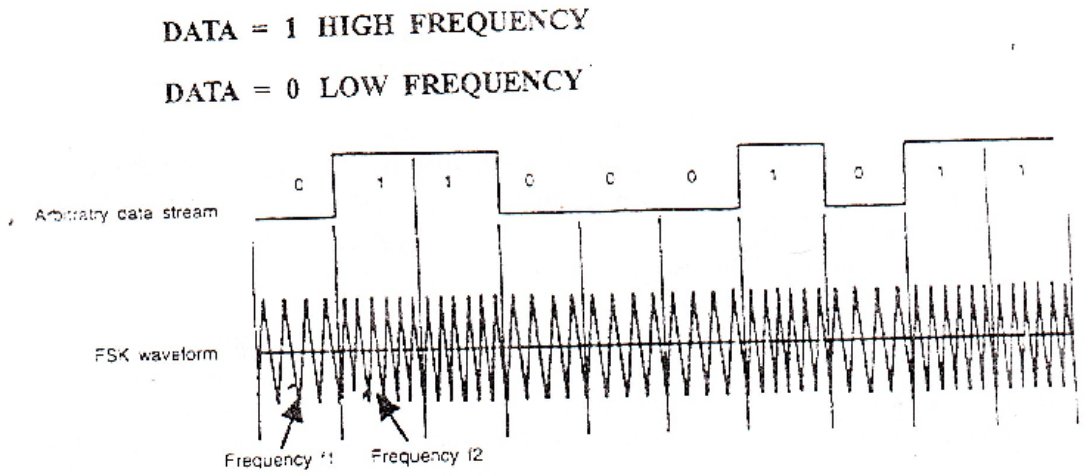
It is also represented as a sum of two ASK signals. The two carriers have different frequencies & the digital data is inverted. The demodulation of FSK can be carried out by a PLL. As known, the PLL tries to 'lock' the input frequency. It achieves this by generating corresponding O/P voltage to be fed to the VCO, if any frequency deviation at its I/P is

encountered. Thus the PLL detector follows the frequency changes and generates proportional O/P voltage. The O/P voltage from PLL contains the carrier components. Therefore to remove this, the signal is passed through Low Pass Filter. The resulting wave is too rounded to be used for digital data processing. Also, the amplitude level may be very low due to channel attenuation.

Procedure:

1. Turn ON the trainer kits. Monitor NRZ(L) O/P (t.p.5) from ST2106 trainer on one channel of the CRO. Use the other channel to monitor the O/P of modulator 1 (t.p. 28) in ST2106 trainer.
2. Observe the O/P of the summing amplifier on the ST 2106 trainer at t.p. 36. Note that it is the FSK waveform for the given data. Adjust the GAIN control of modulator 2, if necessary to make the amplitude of two frequency components equal.
3. Display the FSK waveform simultaneously with NRZ(L) O/P. Observe that, for data bit '0' the FSK signal is at lower frequency (960 Khz) & for bit '1', the FSK signal is at higher frequency (1.44 Mhz).
4. Now, to study about demodulator, examine the input (t.p 16) & the O/P (t.p 17) of ST 2107 FSK demodulator. The PLL detector has been used as the FSK demodulator.
5. The unwanted frequency component is removed by passing it through the LPF. On a dual trace oscilloscope examine the I/P (t.p 23) & O/P (t.p 24) of ST 2107 LPF1 simultaneously. Observe that the O/P contains no carrier frequency components.
6. The rounded O/P of the LPF is removed by passing it through the Data Squaring Circuit but prior to it, the BIAS level of the comparator1 is to be adjusted to a value until the O/P pulse width (t.p 47) is same as the NRZ(L) input t.p 5 on ST2106.

Observations:



FSK WAVEFORM

Result:

The FSK modulator and demodulator circuit has been studied.

Precautions:

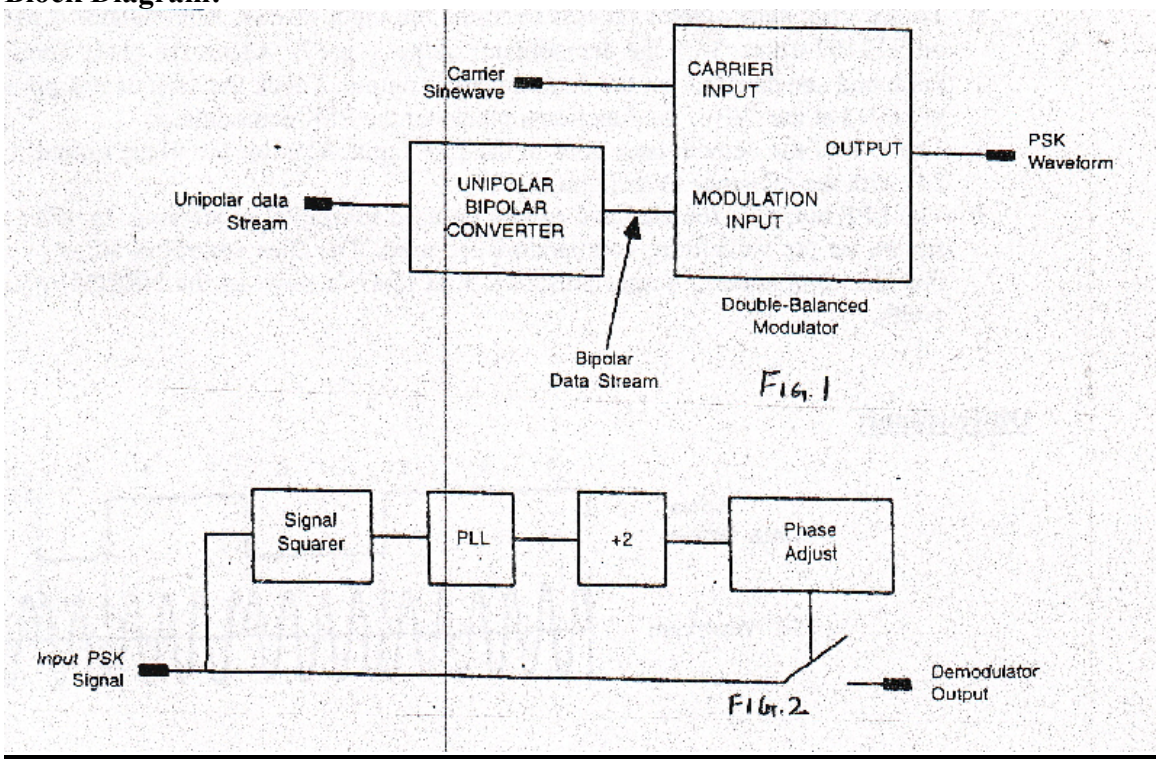
1. Check the connections before switching ON the kit.
2. Observations should be taken properly.

EXPERIMENT No. : 08

Aim: Study of Phase Shift Keying Modulator and Demodulator.

Apparatus Used: PSK Modulator/Demodulator Trainer kit, Binary Data Generator, CRO, CRO probes.

Block Diagram:



Theory: -

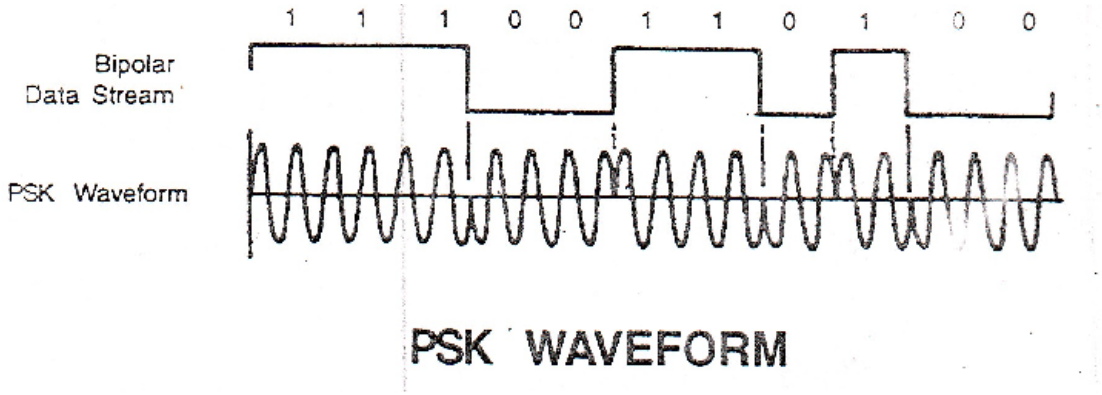
Phase shift keying involves the phase change of the carrier sine wave between 0 and 180 in accordance with the data stream to be transmitted. PSK is also known as Phase reversal keying. PSK modulator is shown in figure 1. Functionally, the PSK modulator is very similar to the ASK modulator. Both uses balanced modulator to multiply the carrier with the modulating signal. But in contrast to ASK techniques, the digital signal applied to the modulator input for PSK generation is bipolar i.e. have equal +ve and –ve voltage levels. The unipolar – bipolar converter converts the unipolar data stream to bipolar data. At receiver, the square loop detector circuit is used to demodulate the transmitted PSK signal. The demodulator is shown in

figure 2. The incoming PSK signal with 0 & 180 phase changes is first fed to the signal square, which multiplies the input signal by itself. The phase adjust circuit allows the phase of the digital signal to be adjusted w.r.t the input PSK signal. Also its O/P controls the closing of an analog switch. When the output is high the switch closes and the original PSK signal is switched through the detector.

Procedure:

1. Connections to be done on ST2106 trainer:
2. Carrier input of modulator 1 to 960 Khz carrier
3. NRZ(M) output t.p 6 to unipolar-bipolar converter input
4. Unipolar-bipolar converter output tp modulator1 input.
5. Connections between ST2106 & ST2107 trainers: Modulator 1 output (t.p. 28) to PSK demodulator input (t.p 10).
6. Connections on ST2107 trainer:
7. PSK demodulator output (t.p 15) to LPF input (t.p.13)
8. LPF output (t.p24) to comparator input (t.p 46)
9. Comparator output (t.p 47) to bit decoder input (t.p 39)
10. Switch ON the trainer kits and monitor the modulator output (t.p 28) in ST2106 trainer with reference to its input (t.p27) by using a dual trace CRO.
11. To see PSK demodulator process examine the input of PSK demodulator (t.p10) on ST2107 trainer with the demodulator output (t.p 15). Adjust the phase control knob and see its effect on the demodulator's output. Check the various test points provided at the O/P of the functional blocks of the PSK demodulator.
12. The O/P of the demodulator goes to the LPF input. Monitor the filters output (t.p 24) with the reference to its input (t.p 28)
13. The LPF output is rounded and cannot be used for digital processing. In order to square up the waveform, comparators are used. The Bias control is adjusted so that the comparator's output pulse width at t.p47 is same as the NRZ(M) pulse width.

Observations:



PSK WAVEFORM

Result:

The PSK modulator and demodulator circuit has been studied.

Precautions:

1. Check the connections before switching ON the kit.
2. Observations should be taken properly.

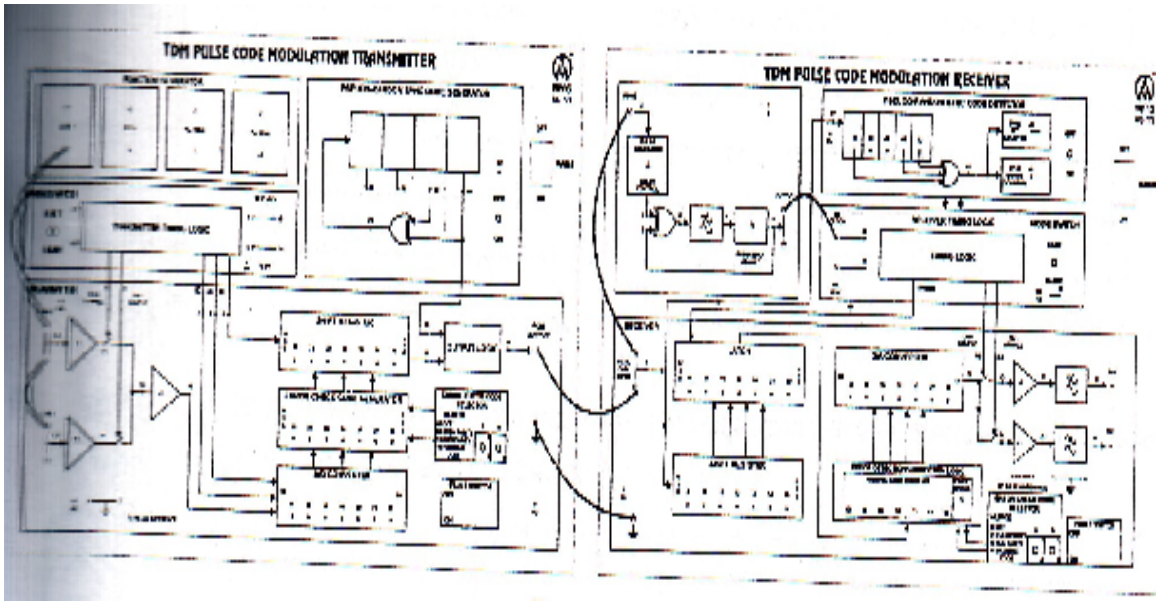
EXPERIMENT No. : 09

Aim: Detection and Correction of Errors using Hamming Code.

Apparatus Used:

1. TDM PCM modulation / demodulation trainer kit.
2. Connecting wires.
3. CRO

Connection Diagram:



Theory: Hamming Code decodes each word at transmitter into a new code by stuffing the word with extra redundant bit. As the name suggests, the redundant bits do not convey information but also provides a method of allowing the receiver to decide when an error has occurred & which bits is in error since the system is binary, the bit in error is easily corrected. Three bit hamming code provides single bit error detection and correction. The kit involves the use of a 7-bit word. Therefore only four bits are used for transmitting data if hamming code is selected. The format becomes: D6 D5 D4 D3 C2 C1 C0
Where, C2, C1 and C0 are hamming code bits.

Procedure:

1. Set up the following initial conditions on TDM-PCM transmitter kit:
    a) Mode switch in FAST position.
    b) DC1 & DC2 amplitude controls in function generator block in fully clockwise position.
    c) Set 1 Khz and 2 Khz signal levels in function generator block to 10 Vpp.
    d) Pseudo-Random syn code generator switched ON.
    e) Error check code selector switches A & B in A=0 & B=0 position.
    f) All switched faults off.
2. Set up the following initial conditions on TDM-PCM receiver kit:
    a) Mode switch in FAST position.
    b) Pseudo-Random syn code generator switched ON.
    c) Error check code selector switches A & B in A=0 & B=0 position.
    d) All switched faults off.
    e) Pulse generator delay adjusts control in fully clockwise position.
3. On TDN-PCM Tx kit connect DC output to CH 0 input (tp 10) and CH 0 (tp 10) input to CH 1 (tp 12) input to ensure that the two channels contain the same information.
4. On TDM-PCM Rx kit connect PCM data input (tp 1) to clock regeneration circuit input (tp 3) and output of clock regeneration circuit (tp 8) to Rx clock input (tp 46).
5. Connect PCM output (tp 44) of Tx kit to PCM data input (tp1) of Rx kit. Also connect the grounds of both the kits.
6. Turn On the power. Ensure that the frequency of the VCO in the receiver clock regeneration circuit has been correctly adjusted.
7. Connect channel 1 of CRO to tp 10 on Tx kit and channel 2 of CRO to tp 33 on Rx kit.
8. Vary DC 1 and note that the data is transferred correctly between the two trainers. This can be verified if the data in the A/D converter blocks of both the kits is same.
9. Select even parity with error check code selector switches A & B at A=0 & B=1 position on both the kits. Set up various codes from A/D converter's output LED's some containing even no. of 1's & some odd. Check the output of error check code generator output on Tx kit, data latch output (tp 16 & tp 22) & D/A converter input (tp 23 & tp 29) on Rx kit.
10. Compare the output of tha data latch LED (tp 16 & tp 22) with input to the D/A converter LED in each case. Once the error detection logic has decided whether an error has occurred, it must pass the received code to D/A converter. But since D0 bit was used as parity bit, it is always forced to a '0'.
11. Set up the error check selector switches to A=1 & B=0 position on both trainers to select the odd parity mode. Repeat steps 9 & 10, but with odd parity as selection.
12. Carry out the same experiment with 1 Khz sine wave applied at CH 0 & CH 1 input of Tx kit. Adjust the 1 Khz amplitude fully clockwise.
13. Switch ON the hamming code error check mode on the kit. Disconnect the sine wave and connect the DC output from the function generator block to CH 0 and CH 1.Adjust the DC control such that the A/D converter's output LED's show 110100 on D6-D0 bits. Note the binary code on the error check code generator..
14. Vary the DC control such that output of A/D converter goes from 1101000 to 1101111. Notice the changes in the binary code output of the error check code. Observe that the error check code generator is only concerned with checking bits D6, D5, D4, D3 only. D2, D1, D0 outputs from A/D converter are ignored by the error check code generator in hamming code as parity check bits C2, C1 and C0 are output in their place depending

on the value of D6, D5, D4, D3 bits. It is for this reason that C2, C1 and C0 bits do not change although the data at D2, D1, and D0 have changed.

Observations:

S No.	Data Received	Case 1 D6 D5 D4 C2	Case 2 D6 D5 D3 C1	Case 3 D6 D4 D3 C0	Bit in Error	Corrected Output
1.	0101011					
2.	0110001					
3.	1101101					
4.	1101001					

Result:

Error detection and correction using Hamming Code has been verified.

Precautions:

1. Check the connections before switching ON the kit.
2. Observations should be taken properly.