Department of Computer Science &

Engineering

LAB MANUAL

SUBJECT: BTCS404(Microprocessor& Assembly Language Programming)

B.Tech 2nd YEAR CSE branch

KCT COLLEGE OF ENGG & TECH,FATEHGARH
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Experiment 1

Apparatus

8085 IC, microprocessor kit, and power supply.

Theory

Intel 8085 is an 8-bit microprocessor. It is 40-pin IC package fabricated on a single LSI chip. It uses a single +5 V supply. Its clock speed is about 3 MHz. It consists of three main sections: -

1.ALU (Arithmetic and logic unit):-

The ALU performs the arithmetic and logical operation, addition, subtraction, logical AND, OR, EX-OR, Complement, Increment, Decrement, shift, clear.

2.Timing and Control Unit:-

It generates timing and control signals, which are necessary for the execution of instruction.

3.Registers: -

These are used for temporary storage of data and instruction. INTEL 8085 has following registers: -

i) One 8 bit accumulator
ii) Six 8 bit registers (B, C, D, E, H, L)
iii) One 16 bit stack pointer, SP
iv) One 16 bit program counter, PC
v) Instruction register
vi) Status register
vii) Temporary registers

PC contains the address of next instruction.
IR holds the instruction until it is decoded.
SP holds the address of the stack top.
Accumulator is used during execution of program for temporary storage of data.

Status flags are as follows: -

i) Carry (CS)
ii) Zero (Z)
iii) Sign (S)
iv) Parity (P)
v) Auxiliary Carry (AC)

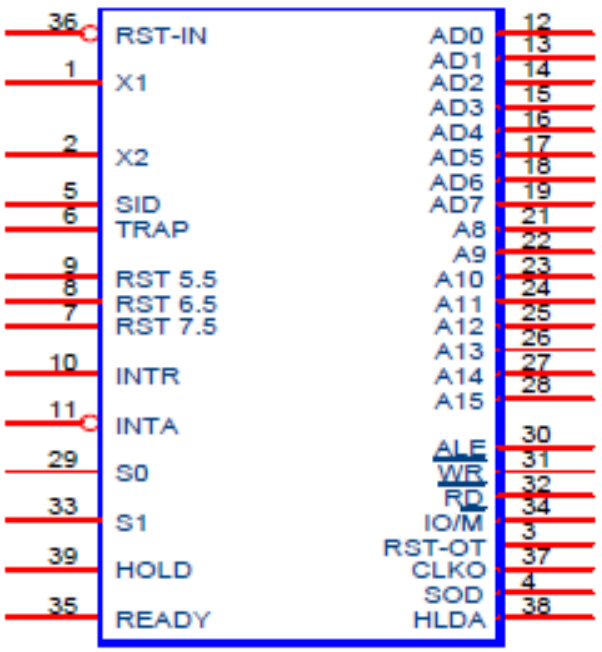
PSW

This 8-bit program status word includes status flags and three undefined bits.

Data and Address bus

Data bus is 8- bit wide and 8 bits of data can be transmitted in parallel. It has 16-bit wide address bus as the memory addresses are of 16 bits.

Circuit Diagram(Pin Diagram):-



Pin Configuration

A8-A15 (Output):-

These are address bus and used for the most significant bits of memory address.

AD0-AD7 (Input/Output):-

These are time multiplexed address data bus. These are used for the least significant 8 bits of the memory address during first clock cycle and then for data during second and third clock cycle

ALE (Address Latch Enable)

It goes high during the 1st clock cycle of a machine. It enables the lower 8 bits of address to be latched either in the memory or external latch.

IO/M

It is status signal, when it goes high; the address on address bus is for I/O device, otherwise for memory.

So, S1

These are status signals to distinguish various types of operation

S1	So	Operation
0	0	Halt
0	1	Write
1	0	Read
1	1	Fetch

RD (output)

It is used to control read operation.

WR (output)

It is used to control write operation.

HOLD (input)

It is used to indicate that another device is requesting the use of address & data bus.

HLDA (output)

It is acknowledgement signal used to indicate HOLD request has been received.

INTR (input)

When it goes high, microprocessor suspends its normal sequence of operations.

INTA (output)

It is interrupt acknowledgement signal sent by microprocessor after INTR is received.

RST 5.5,6.5,7.5 and TRAP

These are various interrupt signals. Among them TRAP is having highest priority

RESET IN (input)

It resets the PC to zero.

RESET OUT(output)

It indicates that CPU is being reset.

X1, X2 (input)

This circuitry is required to produce a suitable clock for the operation of microprocessor.

Clk (output)

It is clock output for user. Its frequency is same at which processor operates.

SID (input)

It is used for data line for serial input.

SOD (output)

It is used for data line for serial output.

Vcc

+5 volts supply

Vss

Ground reference

Experiment No. 2(a)

Aim

Write a well-documented program using 8085 for addition of two 8-bit numbers.

Apparatus

8085 microprocessor kit,5 V power supply, Connecting leads.

Theory (Program)

MEMORY ADDRESS	MACHINE CODE	MNEMONICS	OPERANDS	COMMANDS
7000	21,01,75	LXI	H,7501	Get address of 1st no. in HL pair
7003	7E	MOV	A,M	Move Ist no. in accumulator
7004	23	INX	H	HL points the address 7502H
7005	86	ADD	M	Add the 2nd no.
7006	23	INX H		HL points 7503H
7007	77	MOV	M,A	Store result in 7503H.
7008	CF	RST 1		Terminate

Input Data 7501-
7502-

Output Data
7503-

Experiment No. 3(a)

Aim-

Write a well-documented program using 8085 for substraction of two 8-bit numbers.

Apparatus-

8085 microprocessor kit, 5 V power supply, connecting leads.

Theory(Program)-

Memory address	Opcode	Mnemonics	Operands	Comments
7000	21,01,75	LXI	H, 7501	Get address of ist no. in HL pair
7003	7E	MOV	A, M	Move Ist no. in accumulator
7004	23	INX	H	HL points 7502H.
7005	96	SUB	M	Substract 2nd no. from Ist no.
7006	23	INX	H	HL points 7503 H.
7007	77	MOV	M, A	Move contents of acc. to memory
7008	CF	RST 1		Stop

Input Data 7501-
7502-

Output Data
7503-

Experiment 4

Aim: Write a program to find 1's compliment of 8- bit number.

Apparatus: 8085 microprocessor kit, 5 V power supply, Connecting leads**.**

Program:

Address	Mnemonics	Operand	Opcode	Remarks
2000	LDA	3000H	3A	Load H-L pair with data from 3000H.
2001			00	Lower-order of 3000H.
2002			30	Higher-order of 3000H.
2003	CMA		2F	Complement accumulator.
2004	STA	3001H	32	Store the result at memory location 3001H.
2005			01	Lower-order of 3001H.
2006			30	Higher-order of 3001H.
2007	HLT		76	Halt.

Output:

Before Execution:

3000H: 85H

After Execution:

3001H: 7AH

Experiment 5

Aim: Write a program to find 2's compliment of 8- bit number.

Apparatus: 8085 microprocessor kit, 5 V power supply, Connecting leads**.**

Program:

Address	Mnemonics	Operand	Opcode	Remarks
2000	LDA	3000H	3A	Load H-L pair with data from 3000H.
2001			00	Lower-order of 3000H.
2002			30	Higher-order of 3000H.
2003	CMA		2F	Complement accumulator.
2004	INR	A	2C	Increment accumulator.
2005	STA	3001H	32	Store the result at memory location 3001H.
2006			01	Lower-order of 3001H.
2007			30	Higher-order of 3001H.
2008	HLT		76	Halt.

Output:

Before Execution:

3000H: 85H

After Execution:

3001H: 7BH

Experiment 6

Aim: Shift an 8 bit no. by one bit.

Apparatus: 8085 microprocessor kit, 5 V power supply, Connecting leads**.**

Program:

Address	Mnemonics	Operand	Opcode	Remarks
2000	LDA	3000H	3A	Load H-L pair with data from 3000H.
2001			00	Lower-order of 3000H.
2002			30	Higher-order of 3000H.
2003	RAL		17	Shift left accumulator.
2004	STA	3001H	32	Store the result at memory location 3001H.
2005			01	Lower-order of 3001H.
2006			30	Higher-order of 3001H.
2007	HLT		76	Halt.

Output:

Before Execution:

3000H: 05H

After Execution:

3001H: 0AH

Experiment 7

Aim: Find Largest of two 8 bit numbers.

Apparatus: 8085 microprocessor kit, 5 V power supply, Connecting leads**.**

Program:

Address	Mnemonics	Operand	Opcode	Remarks
2000	LXI	H, 3000H	21	Load H-L pair with address 3000H.
2001			00	Lower-order of 3000H.
2002			30	Higher-order of 3000H.
2003	MOV	A, M	7E	Move the 1st operand from memory to reg. A.
2004	INX	H	23	Increment H-L pair.
2005	MOV	B, M	46	Move the 2nd operand from memory to reg. B.
2006	CMP	B	B8	Compare B with A.
2007	JNC	200BH	D2	Jump to address 200BH if there is no carry.
2008			0B	Lower-order of 200BH.
2009			20	Higher-order of 200BH.
200A	MOV	A, B	78	Move largest from reg. B to reg. A.
200B	INX	H	23	Increment H-L pair.
200C	MOV	M, A	77	Move the result from reg. A to memory.
200D	HLT		76	Halt.

Output:

Before Execution:

3000H: 25H

3001H: 15H

After Execution:

3002H: 25H

Experiment 8

Aim: Find Largest among an array of ten numbers (8 bit).

Apparatus: 8085 microprocessor kit, 5 V power supply, Connecting leads**.**

Memory Address	Machine Code	Mnemonics	Comments
7000	21,00,75	LXI H, 7500 H	Address for count in H-L pair
7003	4E	MOV C, M	Count in register C
7004	23	INX H	Address of Ist number in HL pair
7005	7E	MOV A,M	Ist no. in accumulator
7006	0D	DCR C	Decrement count
7007	23 Loop	INX H	Address of next number
7008	BE	CMP M	Is next number>previous no.
7009	D2,0D,70	JNC Ahead	If not carry,jump to ahead
700C	7E	MOV A,M	Get larger no. into acc.
700D	0D Ahead	DCR C	Decrement count
700E	C2,07,70	JNZ Loop	
7011	32,50,74	STA 7450 H	Store result at 7450.
7014	CF	RST 1	Terminate.

Input Data 7500-03 (Counter)
7501-
7502-
7503-

Output Data
7450-

Experiment 9

Aim: Sum of series of 8 bit numbers.

Apparatus: 8085 microprocessor kit, 5 V power supply, Connecting leads**.**

Program:

Address	Mnemonics	Operand	Opcode	Remarks
2000	LXI	H, 3000H	21	Load H-L pair with address 3000H.
2001			00	Lower-order of 3000H.
2002			30	Higher-order of 3000H.
2003	MOV	C, M	4E	Move counter from memory to reg. C.
2004	MVI	A, 00H	3E	Initialize accumulator with 00H.
2005			00	Immediate value 00H.
2006	INX	H	23	Increment H-L pair.
2007	MOV	B, M	46	Move next number from memory to reg. B.
2008	ADD	B	80	Add B with A.
2009	DCR	C	0D	Decrement counter.
200A	JNZ	2006H	C2	Jump to address 2006H if counter is not zero.
200B			06	Lower-order of 2006H.
200C			20	Higher-order of 2006H.
200D	INX	H	23	Increment H-L pair.
200E	MOV	M, A	77	Move the result from reg. A to memory.
200F	HLT		76	Halt.

Output:

Before Execution:

3000H: 05H (Counter)

3001H: 02H

3002H: 04H

3003H: 03H

3004H: 02H

3005H: 01H

After Execution:

3006H: 0CH

Experiment 10

Apparatus: 8086 microprocessor kit, 5 V power supply, Connecting leads**.**

Introduction The 8086 trainer kit is built around the Intel 8086 microprocessor (CPU). It contains simple keypad for interning commands and data, a simple 7 — segment display unit for displaying data and result, a monitor program contained in (4k byte **)** of EPROM and (2k byte **)** RAM and input / output ports • The monitor program contains all necessary subroutines for the operation of the keypad and display, as well as some other useful functions.

The 8086 registers The 8086 use a group of registers for most data manipulation tasks. These registers play an important role in programming the 8086. Figure (1) shows the 8086 registers that can be accessed by the user. Here is a brief description of each register. 1- Instruction pointer (IP): This (16 — bit) register identify the location of the next word of instruction code to be fetched from the current code segment of memory . The value of the address for the next code access is often denoted as CS : IP.

2- Data registers: These are (16 — bit) four general purpose registers and they are reflected to as the accumulator (A), the base register (B), the count register (C), and the data register (D). Each of these registers can be accessed either as a whole (16 — bit) and denoted as (AX ,BX , CX, DX) or as an (8 — bit) and denoted as (AL, AH, BL, BH, CL, CH, DL DR) . They are used for temporary storage of frequently used immediate result.

3- Pointer and index registers (DI, SI ,BP, SP): These (16 — bit) registers shown in fig (1) are two pointer registers (BP (base pointer) , SP (stack pointer)). And two index registers (DI (destination index), SI (source index)). They are used to storage the offset address.

4- Status register (SR): Is a (16 — bit) register also called the flag register. Just nine of its bits are implemented. Six of these are (ZF) zero flag (CF) carry flag, (OF) overflow flag, (AF) auxiliary carry flag , (PF) parity flag, (SF) sign flag and three control flag: (DF) direction flag, (IF) interrupt enable flag and (TP) trap flag . The logic states of these are produced as the result of executing an instruction, such as ADD.

5- Segment register: These are (16 — bit) four registers, code segment (CS), stack segment (SS), data segment (DS) and extra segment (ES) each of these registers contair

points to the lowest addressed byte of the segment in memory. And give a maximum of 256k byte of active memory.

8086 data transfer instruction

The instruction of the microprocessor defines the basic operations that a programmer can specify to the device to perform. The 8086 move data from place to place in the system using a group of data transfer instruction. These instructions provided to move data either between its internal registers or between an internal register and a storage location in memory. A summary of several 8086 data transfer instruction is given below:

MOV, XCHG, XLAT,LEA etc.

This status register contains six status flag and three control flag.

The function of these status flag are outlined below:

1-Carry flag (CF): this flag is set whenever there is a carry out, either from d7 after an 8-bit operation or from d15 after a 16-bit data operation.

2- Parity flag (P0: after certain operations the parity of the results low- order byte is checked, if the byte has an even no. of iS ,the parity flag is set.

3- Auxiliary carry flag (AF):- if there is a carry from d3 to d4 of an operation, this bit is set, other wise, it is cleared. Used for BCD instruction.

4- Zero — flag (ZF):- the Zero-flag is set to 1 if the result of an arithmetic or logic operation is Zero.

5- Sign flag (SF):- binary representation of signed number uses the M.S.B as the sign bit. After arithmetic operation the SF represent the sign of the result.

6- Over flow (OF):-this flag is set whenever the result of a signed number operation is too large, causing the high-order bit to over flow into the sign bit.

Experiment 11

Aim: Addition of two 16 bit numbers.

Apparatus: 8085 microprocessor kit, 5 V power supply, Connecting leads**.**

Program:

Address	Mnemonics	Operand	Opcode	Remarks
2000	LHLD	3000H	2A	Load H-L pair with 1st operand from 3000H.
2001			00	Lower-order of 3000H.
2002			30	Higher-order of 3000H.
2003	XCHG		EB	Exchange H-L pair with D-E pair.
2004	LHLD	3002H	2A	Load H-L pair with 2nd operand from 3002H.
2005			02	Lower-order of 3002H.
2006			30	Higher-order of 3002H.
2007	DAD	D	19	Add D-E pair with H-L pair.
2008	SHLD	3004H	22	Store the result at address 3004H.
2009			04	Lower-order of 3004H.
200A			30	Higher-order of 3004H.
200B	HLT		76	Halt.

Output:

Before Execution:

3000H: 02H

3001H: 04H

3002H: 04H

3003H: 03H

After Execution:

3004H: 06H

3005H: 07H

Experiment 12

Aim: Subtraction of two 16 bit numbers.

Apparatus: 8085 microprocessor kit, 5 V power supply, Connecting leads**.**

Program:

Address	Mnemonics	Operand	Opcode	Remarks
2000	LHLD	3000H	2A	Load H-L pair with 1st operand from 3000H.
2001			00	Lower-order of 3000H.
2002			30	Higher-order of 3000H.
2003	XCHG		EB	Exchange H-L pair with D-E pair.
2004	LHLD	3002H	2A	Load H-L pair with 2nd operand from 3002H.
2005			02	Lower-order of 3002H.
2006			30	Higher-order of 3002H.
2007	MOV	A, E	7B	Move the lower-order of 1st number from reg. E to reg. A.
2008	SUB	L	95	Subtract the lower-order of 2nd number from lower-order of 1st number.
2009	MOV	L, A	6F	Move the result from reg. A to register L.
200A	MOV	A, D	7A	Move the higher-order of 1st number from reg. D to reg. A.
200B	SBB	H	9C	Subtract the higher-order of 2nd number from higher-order of 1st number with borrow from the previous subtraction.
200C	MOV	H, A	67	Move the result from reg. A to reg. H.
200D	SHLD	3004H	22	Store the 16-bit result from H-L pair to memory.
200E			04	Lower-order of 3004H.
200F			30	Higher-order of 3004H.
2010	HLT		76	Halt.

Output:

Before Execution:

3000H:	08H
3001H:	06H
3002H:	05H
3003H:	04H

After execution:

3004H:	03H
3005H:	02H

Experiment 13

Aim: Write a program to find 1's compliment of 16- bit number.

Apparatus: 8085 microprocessor kit, 5 V power supply, Connecting leads**.**

Address	Mnemonics	Operand	Opcode	Remarks
2000	LHLD	3000H	2A	Load H-L pair with operand from 3000H.
2001			00	Lower-order of 3000H.
2002			30	Higher-order of 3000H.
2003	MOV	A, L	7D	Move the lower-order from reg. L to reg. A.
2004	CMA		2F	Complement accumulator.
2005	MOV	L, A	6F	Move the result from reg. A to reg. L.
2006	MOV	A, H	7C	Move the higher-order from reg. H to reg. A.
2007	CMA		2F	Complement accumulator.
2008	MOV	H, A	67	Move the result from reg. A to reg. H.
2009	SHLD	3002H	22	Store the result at address 3002H.
200A			02	Lower-order of 3002H.
200B			30	Higher-order of 3002H.
200C	HLT		76	Halt.

Output:

Before Execution:		**After Execution:**	
3000H:	45H	3002H:	BAH
3001H:	6AH	3003H:	95H

Experiment 14

Aim: Write a program to find 2's compliment of 16- bit number.

Apparatus: 8085 microprocessor kit, 5 V power supply, Connecting leads**.**

Program:

Address	Mnemonics	Operand	Opcode	Remarks
2000	LHLD	3000H	2A	Load H-L pair with operand from 3000H.
2001			00	Lower-order of 3000H.
2002			30	Higher-order of 3000H.
2003	MOV	A, L	7D	Move the lower-order from reg. L to reg. A.
2004	CMA		2F	Complement accumulator.
2005	MOV	L, A	6F	Move the result from reg. A to reg. L.
2006	MOV	A, H	7C	Move the higher-order from reg. H to reg. A.
2007	CMA		2F	Complement accumulator.
2008	MOV	H, A	67	Move the result from reg. A to reg. H.
2009	INX	H	23	Increment H-L pair to find 2's complement.
200A	SHLD	3002H	22	Store the result at address 3002H.
200B			02	Lower-order of 3002H.
200C			30	Higher-order of 3002H.
200D	HLT		76	Halt.

Output:

Before Execution:		**After Execution:**	
3000H:	12H	3002H:	EEH
3001H:	05H	3003H:	FAH