Department of

Electronic & Telecommunication Engineering

LAB MANUAL

VLSI LAB

B.Tech– VI Semester

KCT College OF ENGG AND TECH.

VILLAGE FATEHGARH

DISTT.SANGRUR

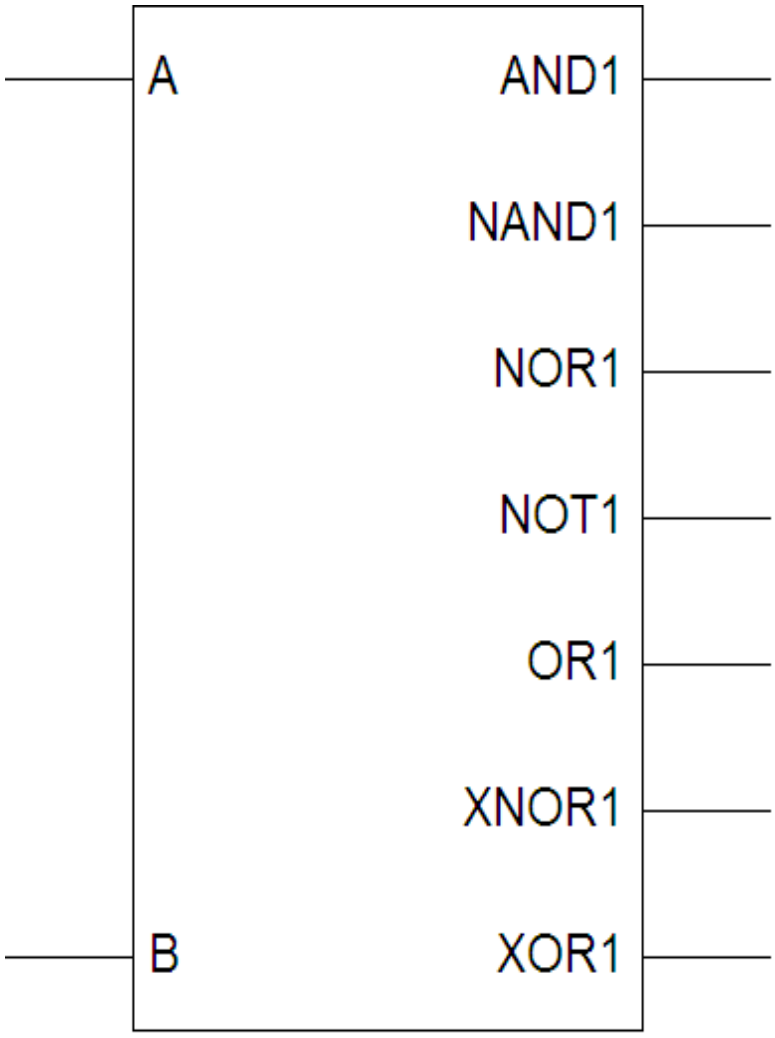
List of Experiments:

1. Design of basic Gates: AND, OR, NOT.
2. Design of universal gates.
3. Design of 8:1 Mux using other basic gates.
4. Design of 2 to 4 Decoder.
5. Design of Half-Adder, Full Adder, Half Substractor, Full Substractor.
6. Design of 3:8 Decoder.
7. Design of 8:3 Priority Encoder.
8. Design of 4 Bit Binary to Grey code Converter.
9. Design of 4 Bit Binary to BCD Converter using sequential statement.
10. Design an 8 Bit parity generator (with for loop and Generic statements).
11. Design of 2,s Complementary for 8-bit Binary number using Generate statements.

Sequential Design Exercises

12. Design of all type of Flip-Flops using (if-then-else) Sequential Constructs.
13. Design of 8-Bit Shift Register with shift Right, Rhisft Left, Load and Synchronous reset.
14. Design of Synchronous 8-bit Johnson Counter.
15. Design of Synchronous 8-Bit universal shift register (parallel-in, parallel-out) with 3-state output (IC 74299)
16. Design of 4 Bit Binary to BCD Converter using sequential statement.
17. Design counters (MOD 3, MOD 5, MOD 8, MOD 16)
18. Design a decimal up/down counter that counts up from 00 to 99 or down from 99 to 00.
19. Design 3-line to 8-line decoder with address latch.

Schematic Diagram:



Experiment No:1&2 Logic Gates

Aim: To Design Logic Gates using VHDL and simulate the same using Xilinx ISE Simulator

Tools Required: 1.PC

2. Xilinx ISE

VHDL Code:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
entity logic_gates is
   Port ( A : in  STD_LOGIC;
          B : in  STD_LOGIC;
          AND1 : out  STD_LOGIC;
          OR1 : out  STD_LOGIC;
          NOT1 : out  STD_LOGIC;
          XOR1 : out  STD_LOGIC;
          NAND1 : out  STD_LOGIC;
          NOR1 : out  STD_LOGIC;
          XNOR1 : out  STD_LOGIC);
end logic_gates;
architecture Behavioral of logic_gates is
begin
AND1<=A AND B;
OR1<=A OR B;
NOT1<=NOT A;
XOR1<=A XOR B;
NAND1<= A NAND B;
NOR1<=A NOR B;
XNOR1<=A XNOR B;
end Behavioral;
```

Synthesis Report

A) Final Report:

Final Results

RTL Top Level Output File Name : logic_gates.ngr

Top Level Output File Name : logic_gates

Output Format : NGC

Optimization Goal : Speed

Keep Hierarchy : NO

B) Design Statistics

IOs : 9

Cell Usage :

BELS : 7

INV : 1

LUT2 : 6

IO Buffers : 9

IBUF : 2

OBUF : 7

==========

Device utilization summary:

Selected Device : 3s250eft256-5

Number of Slices:	4	out of 2448	0%
Number of 4 input LUTs:	7	out of 4896	0%
Number of IOs:	9		
Number of bonded IOBs:	9	out of 172	5%

C) TIMING REPORT:

Delay: 5.998ns (Levels of Logic = 3)
Source: A (PAD)
Destination: NOR1 (PAD)

Data Path: A to NOR1

Cell:in->out	fanout	Gate Delay	Net Delay	Logical Name (Net Name)
IBUF:I->O	7	1.106	0.754	A_IBUF (A_IBUF)
LUT2:I0->O	1	0.612	0.357	OR11 (OR1_OBUF)

OBUF:I->O 3.169 OR1_OBUF (OR1)

Total 5.998ns

VHDL Test bench:

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.std_logic_unsigned.all;
USE ieee.numeric_std.ALL;
ENTITY tb_logic_gates_vhd IS
END tb_logic_gates_vhd;
ARCHITECTURE behavior OF tb_logic_gates_vhd IS
        COMPONENT logic_gates
    PORT(
        A : IN std_logic;
        B : IN std_logic;
        AND1 : OUT std_logic;
        OR1 : OUT std_logic;
        NOT1 : OUT std_logic;
        XOR1 : OUT std_logic;
        NAND1 : OUT std_logic;
        NOR1 : OUT std_logic;
        XNOR1 : OUT std_logic
        );
    END COMPONENT;
    SIGNAL A :  std_logic := '0';
    SIGNAL B :  std_logic := '0';
    SIGNAL AND1 :  std_logic;
```

SIGNAL OR1 : std_logic;

SIGNAL NOT1 : std_logic;

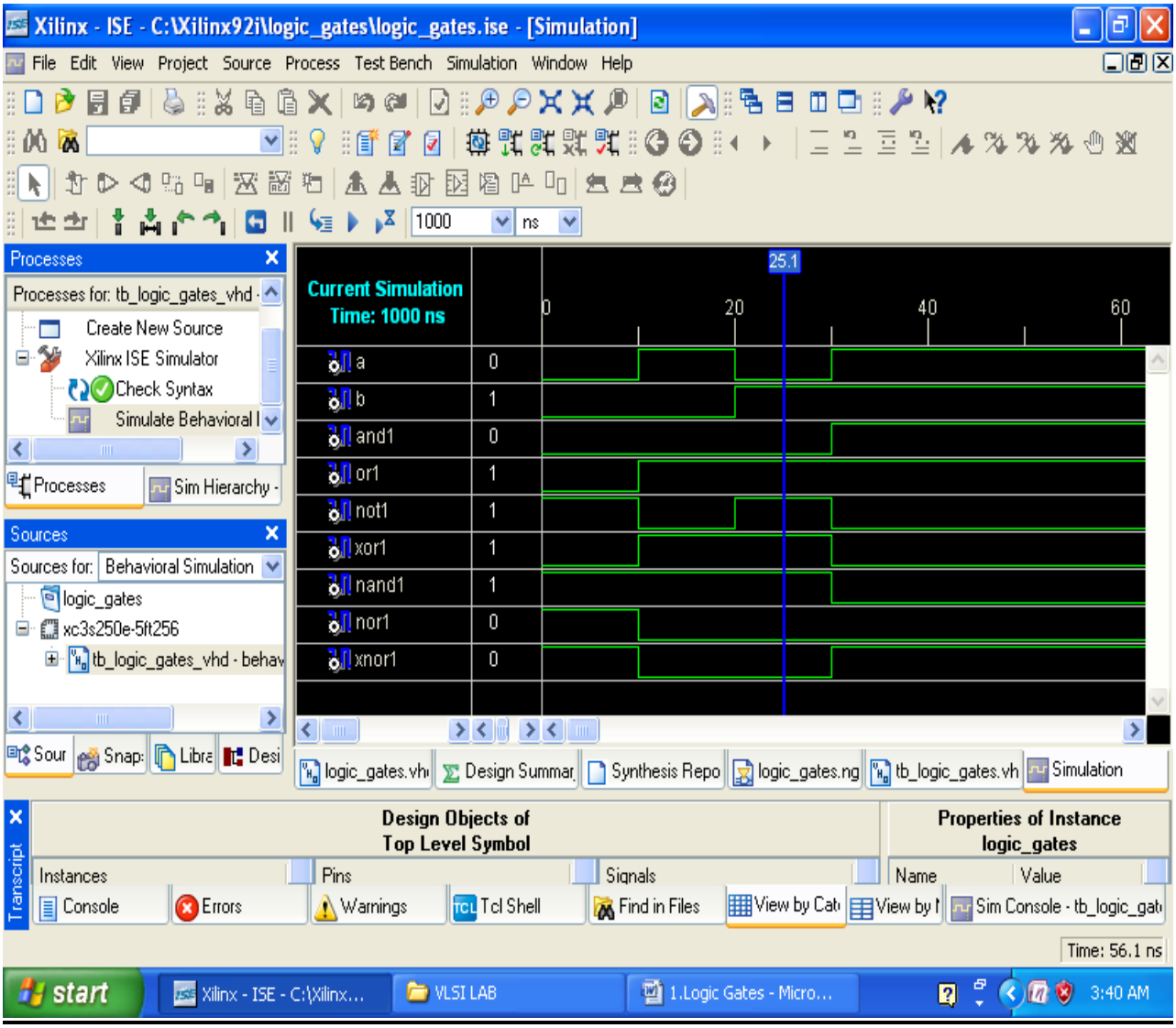
SIGNAL XOR1 : std_logic;

SIGNAL NAND1 : std_logic;

SIGNAL NOR1 : std_logic;

SIGNAL XNOR1 : std_logic;

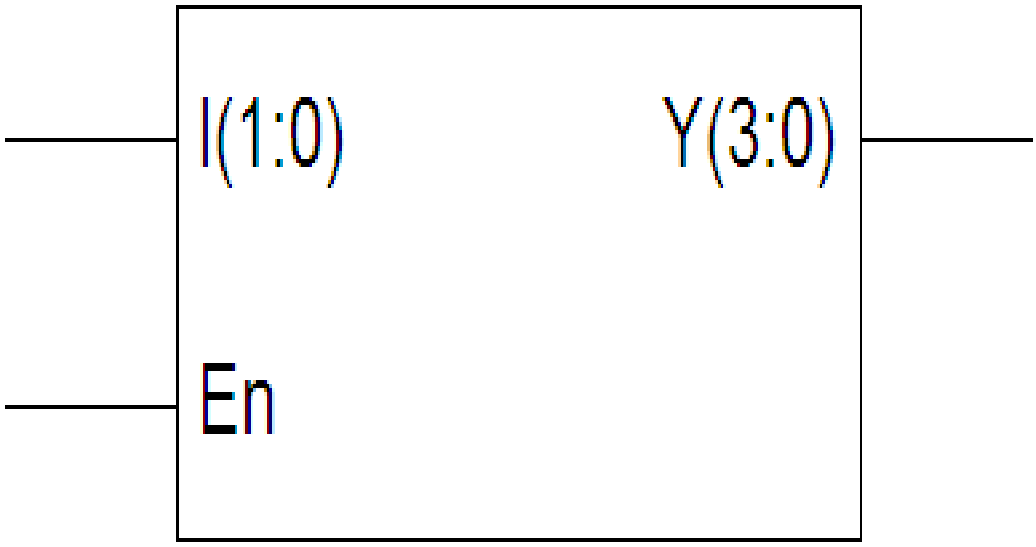
Simulation Results:



```
BEGIN
        uut: logic_gates PORT MAP(
        A => A,
        B => B,
        AND1 => AND1,
        OR1 => OR1,
        NOT1 => NOT1,
        XOR1 => XOR1,
        NAND1 => NAND1,
        NOR1 => NOR1,
        XNOR1 => XNOR1
    );
A<='1' AFTER 10NS,'0' AFTER 20NS,'1' AFTER 30NS;
B<='1' AFTER 20NS;
END;
```

Result: Logic Gates are designed using VHDL and simulated the same using Xilinx ISE Simulator

Schematic Diagram:


I(1:0)
Y(3:0)
En

Experiment No:3 8-To-1 Multiplexer

Aim: To Design **8-To-1 Multiplexer** using VHDL and simulate the same using Xilinx ISE Simulator

Tools Required: 1.PC

2. Xilinx ISE

VHDL Code:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
entity Mux_8_1 is
   Port ( En_L : in  STD_LOGIC;
          S : in  STD_LOGIC_VECTOR (2 downto 0);
          I : in  STD_LOGIC_VECTOR (7 downto 0);
          Y : out  STD_LOGIC);
end Mux_8_1;
architecture Behavioral of Mux_8_1 is
begin
    process(S,I,En_L)
    begin
      if En_L='1' then Y<='0';
     else
           case S is
           when "000"=>Y<=I(0);
           when "001"=>Y<=I(1);
           when "010"=>Y<=I(2);
           when "011"=>Y<=I(3);
           when "100"=>Y<=I(4);
           when "101"=>Y<=I(5);
           when "110"=>Y<=I(6);
```

```
            when "111"=>Y<=I(7);
            when others=>Y<='Z';

              end case;
           end if;
        end process;
    end Behavioral;
```

Synthesis Report

Final Report:

Final Results

RTL Top Level Output File Name : Mux_8_1.ngr

Top Level Output File Name : Mux_8_1

Output Format : NGC

Optimization Goal : Speed

Keep Hierarchy : NO

Design Statistics

IOs : 13

Cell Usage :

BELS : 8

LUT3 : 1

LUT4 : 5

MUXF5 : 2

IO Buffers : 13

IBUF : 12

OBUF : 1

==========

Device utilization summary:

Selected Device : 3s250eft256-5

Number of Slices: 3 out of 2448 0%

Number of 4 input LUTs: 6 out of 4896 0%

Number of IOs: 13

Number of bonded IOBs: 13 out of 172 7%

TIMING REPORT:

Delay: 7.512ns (Levels of Logic = 6)
Source: S<0> (PAD)
Destination: Y (PAD)
Data Path: S<0> to Y

Cell:in->out	fanout	Gate Delay	Net Delay	Logical Name (Net Name)
IBUF:I->O	4	1.106	0.651	S_0_IBUF (S_0_IBUF)
LUT4:I0->O	1	0.612	0.000	Y97_F (N85)
MUXF5:I0->O	2	0.278	0.449	Y97 (Y_map27)
LUT3:I1->O	1	0.612	0.000	Y1241 (N89)
MUXF5:I1->O	1	0.278	0.357	Y124_f5 (Y_OBUF)
OBUF:I->O		3.169		Y_OBUF (Y)
Total	7.512ns			

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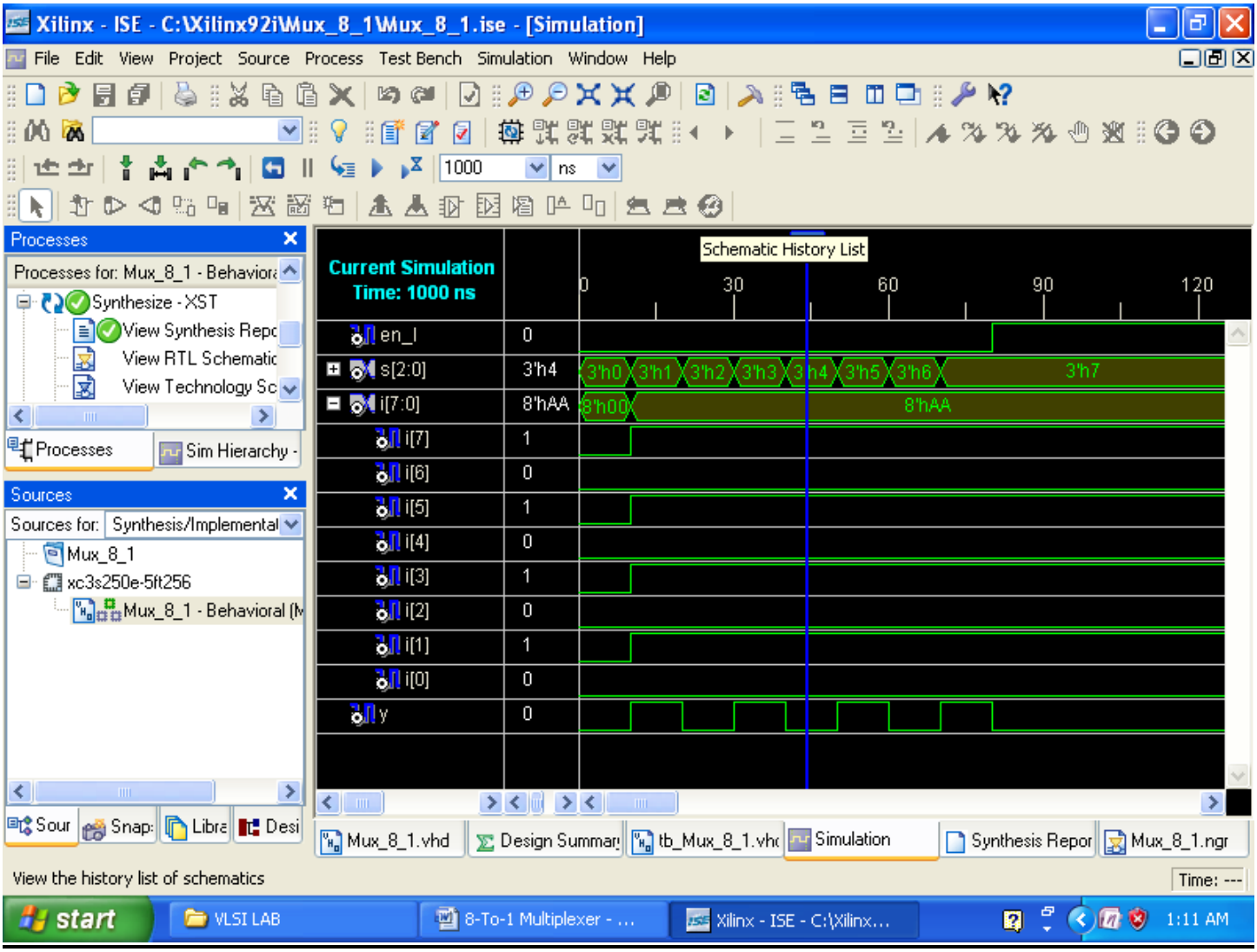
VHDL Test bench:

```
LIBRARY ieee;

USE ieee.std_logic_1164.ALL;

USE ieee.std_logic_unsigned.all;

USE ieee.numeric_std.ALL;

ENTITY tb_Mux_8_1_vhd IS
END tb_Mux_8_1_vhd;
ARCHITECTURE behavior OF tb_Mux_8_1_vhd IS
    COMPONENT Mux_8_1
    PORT(
        En_L : IN std_logic;
        S : IN std_logic_vector(2 downto 0);
        I : IN std_logic_vector(7 downto 0);
        Y : OUT std_logic
        );
    END COMPONENT;
    SIGNAL En_L :  std_logic := '0';
    SIGNAL S :  std_logic_vector(2 downto 0) := (others=>'0');
    SIGNAL I :  std_logic_vector(7 downto 0) := (others=>'0');
```

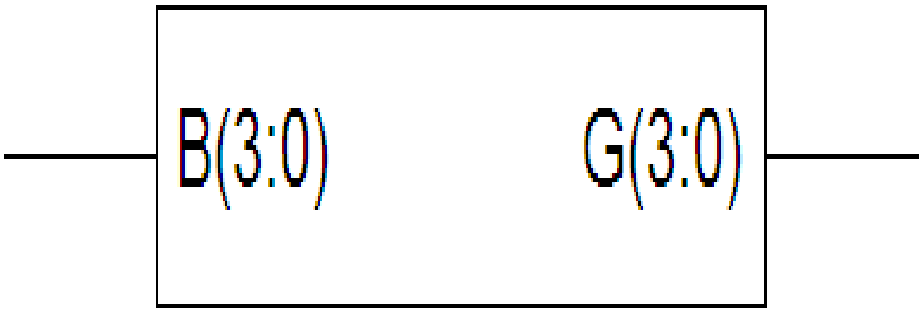
```
        SIGNAL Y :  std_logic;
BEGIN
                uut: Mux_8_1 PORT MAP(
                En_L => En_L,
                S => S,
                I => I,
                Y => Y
        );
        En_L<='1' after 80ns;
I<="10101010" after 10ns;
S<="001" after 10ns,"010" after 20ns,"011" after 30ns,"100" after 40ns,"101" after 50ns,"110" after 60ns,"111" after 70ns;
END;
```

Result: **8-To-1 Multiplexer** is designed using VHDL and simulated the same using Xilinx ISE Simulator.

Simulation Results:



Schematic Diagram:



Synthesis Report

HDL Synthesis Report

Macro Statistics

Xors : 3
1-bit xor2 : 3

Advanced HDL Synthesis Report

Macro Statistics
Xors : 3
1-bit xor2 : 3

Final Report:

RTL Top Level Output File Name : Binary_to_gray.ngr
Top Level Output File Name : Binary_to_gray
Output Format : NGC
Optimization Goal : Speed
Keep Hierarchy : NO

Design Statistics

IOs : 8

Cell Usage :

BELS : 3
LUT2 : 3
IO Buffers : 8
IBUF : 4
OBUF : 4

Device utilization summary:

Selected Device : 3s250eft256-5

Number of Slices: 2 out of 2448 0%
Number of 4 input LUTs: 3 out of 4896 0%
Number of IOs: 8
Number of bonded IOBs: 8 out of 172 4%

TIMING REPORT:

Data Path: B<2> to G<2>

Cell:in->out	fanout	Gate Delay	Net Delay	Logical Name (Net Name)
IBUF:I->O	2	1.106	0.532	B_2_IBUF (B_2_IBUF)
LUT2:I0->O	1	0.612	0.357	Mxor_G<2>_Result1 (G_2_OBUF)
OBUF:I->O		3.169		G_2_OBUF (G<2>)

Experiment No:4 2-To-4 decoder

Aim: To Design **2-To-4 decoder** using VHDL and simulate the same using Xilinx ISE Simulator

Tools Required: 1.PC

2. Xilinx ISE

VHDL Code:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
entity decoder is
   Port ( En : in  STD_LOGIC;
          I : in  STD_LOGIC_VECTOR (1 downto 0);
          Y : out  STD_LOGIC_VECTOR (3 downto 0));
end decoder;
architecture Behavioral of decoder is
begin
     process(En,I)
     begin
         if En='0' then Y<="0000";
         else
           case I is
             when "00" =>Y<="0001";
             when "01" =>Y<="0010";
             when "10" =>Y<="0100";
             when "11" =>Y<="1000";
             when others =>Y<="ZZZZ";
           end case;
  end if;
  end process;
end Behavioral;
```

Synthesis Report

Final Report:

Final Results
RTL Top Level Output File Name : decoder.ngr
Top Level Output File Name : decoder
Output Format : NGC
Optimization Goal : Speed
Keep Hierarchy : NO

Design Statistics

IOs : 7

Cell Usage :

BELS : 4
LUT3 : 4
IO Buffers : 7
IBUF : 3
OBUF : 4

==========

Device utilization summary:

Selected Device : 3s250eft256-5

Number of Slices:	2	out of 2448	0%
Number of 4 input LUTs:	4	out of 4896	0%
Number of IOs:	7		
Number of bonded IOBs:	7	out of 172	4%

TIMING REPORT:

Delay: 5.895ns (Levels of Logic = 3)
Source: I<1> (PAD)
Destination: Y<3> (PAD)

Data Path: I<1> to Y<3>

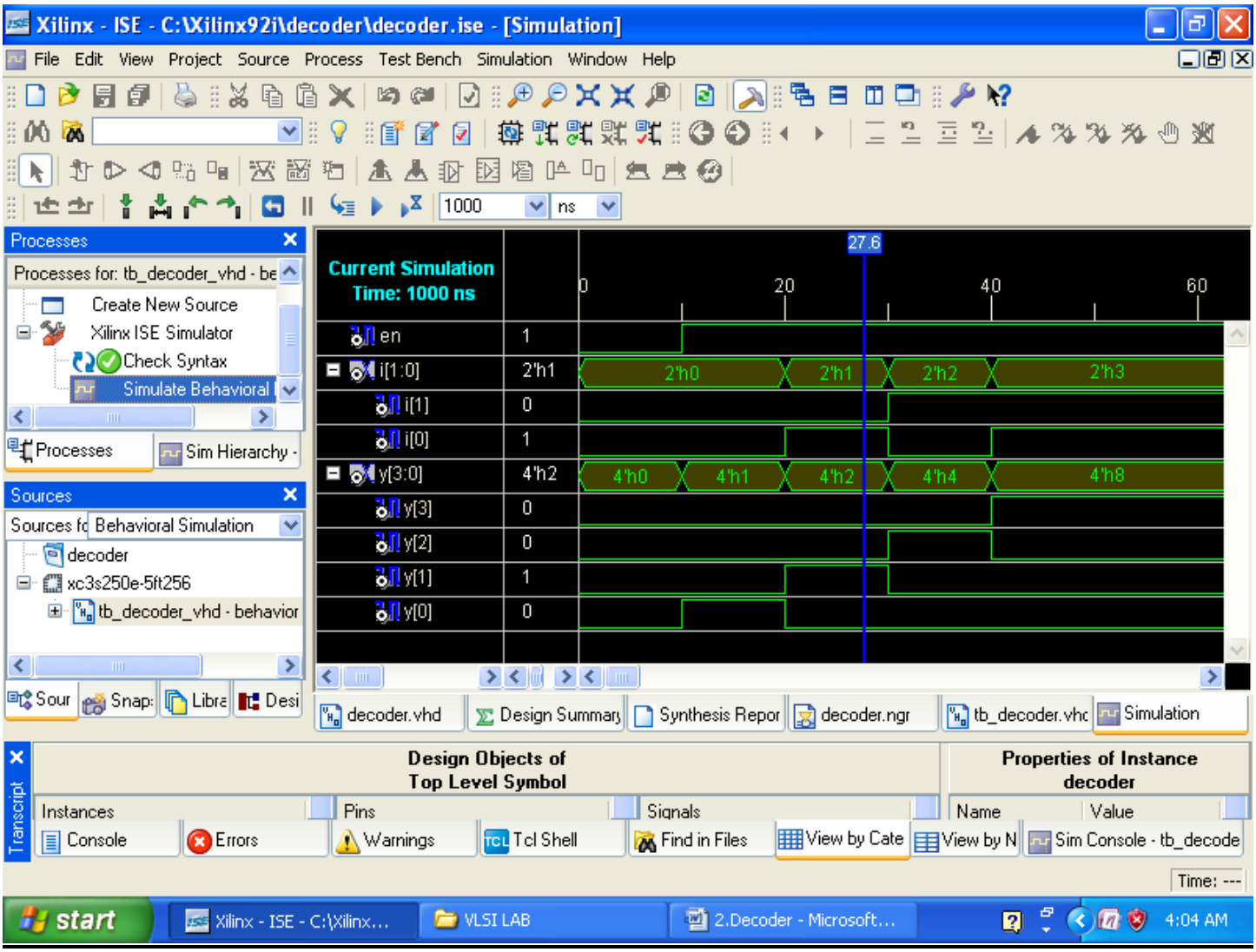
Cell:in->out	fanout	Gate Delay	Net Delay	Logical Name (Net Name)
IBUF:I->O	4	1.106	0.651	I_1_IBUF (I_1_IBUF)
LUT3:I0->O	1	0.612	0.357	Y<3>1 (Y_3_OBUF)
OBUF:I->O		3.169		Y_3_OBUF (Y<3>)
Total		5.895ns		

VHDL Test bench:

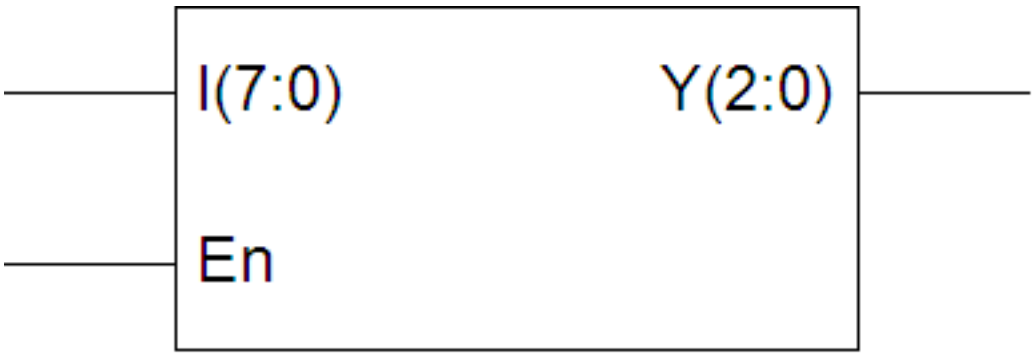
```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.std_logic_unsigned.all;
USE ieee.numeric_std.ALL;
ENTITY tb_decoder_vhd IS
END tb_decoder_vhd;
ARCHITECTURE behavior OF tb_decoder_vhd IS
        COMPONENT decoder
        PORT(
                En : IN std_logic;
                I : IN std_logic_vector(1 downto 0);
                Y : OUT std_logic_vector(3 downto 0)
                );
        END COMPONENT;
        SIGNAL En :  std_logic := '0';
        SIGNAL I :  std_logic_vector(1 downto 0) := (others=>'0');
        SIGNAL Y :  std_logic_vector(3 downto 0);
BEGIN
uut: decoder PORT MAP(
                En => En,
                I => I,
                Y => Y
        );
        En<='1' after 10ns;
        I<="01" after 20ns,"10" after 30ns,"11" after 40ns;
END;
```

Result: 2-To-4 Decoder is designed using VHDL and simulated the same using Xilinx ISE Simulator

Simulation Results:



Schematic Diagram:



Synthesis Report

Final Report:

Final Results
RTL Top Level Output File Name : encoder_without_priority.ngr
Top Level Output File Name : encoder_without_priority
Output Format : NGC
Optimization Goal : Speed
Keep Hierarchy : NO

Design Statistics

IOs : 12

Cell Usage :

BELS : 15
LUT3 : 6
LUT4 : 9
IO Buffers : 12
IBUF : 9
OBUFT : 3

Device utilization summary:

Selected Device : 3s250eft256-5

Number of Slices:	9	out of 2448	0%
Number of 4 input LUTs:	15	out of 4896	0%
Number of IOs:	12		
Number of bonded IOBs:	12	out of 172	6%

TIMING REPORT:

Delay: 9.315ns (Levels of Logic = 6)

Source: I<0> (PAD)

Destination: Y<2> (PAD)

Data Path: I<0> to Y<2>

Cell:in->out	fanout	Gate Delay	Net Delay	Logical Name (Net Name)
IBUF:I->O	4	1.106	0.651	I_0_IBUF (I_0_IBUF)
LUT3:I0->O	2	0.612	0.532	Y_mux0000<0>41 (Y_mux0000<0>_bdd4)
LUT3:I0->O	2	0.612	0.449	Y_not0001_inv21 (Y_not0001_inv_bdd3)
LUT4:I1->O	1	0.612	0.509	Y_not0001_inv59 (Y_not0001_inv_map17)
LUT4:I0->O	3	0.612	0.451	Y_not0001_inv93 (Y_not0001_inv)
OBUFT:T->O		3.169		Y_2_OBUFT (Y<2>)

Experiment No:5(a) Full Adder Using Dataflow Style

Aim: To Design **Full Adder Using Dataflow Style** using VHDL and simulate the same using Xilinx ISE Simulator

Tools Required: 1.PC

2. Xilinx ISE

VHDL Code:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
entity Full_Adder_Dataflow is
   Port ( A : in  STD_LOGIC;
          B : in  STD_LOGIC;
          Cin : in  STD_LOGIC;
          Sum : out  STD_LOGIC;
          Cout : out  STD_LOGIC);
end Full_Adder_Dataflow;
```

```
architecture Dataflow of Full_Adder_Dataflow is
signal X: STD_LOGIC;
begin
X<= (A xor B) and Cin;
Sum<= A xor B xor Cin;
Cout<=X or (A and B);
end Dataflow;
```

Synthesis Report

HDL Synthesis Report:

Macro Statistics
Xors : 2
1-bit xor2 : 2

Final Report:

Final Results
RTL Top Level Output File Name : Full_Adder_Dataflow.ngr
Top Level Output File Name : Full_Adder_Dataflow
Output Format : NGC
Optimization Goal : Speed
Keep Hierarchy : NO
Design Statistics
IOs : 5
Cell Usage :
BELS : 2
LUT3 : 2
IO Buffers : 5
IBUF : 3
OBUF : 2
Device utilization summary:
Selected Device : 3s250eft256-5

Number of Slices: 1 out of 2448 0%
Number of 4 input LUTs: 2 out of 4896 0%
Number of IOs: 5
Number of bonded IOBs: 5 out of 172 2%

TIMING

Delay: 5.776ns (Levels of Logic = 3)

Source: B (PAD)

Destination: Cout (PAD)

Data Path: B to Cout

Cell:in->out	fanout	Gate Delay	Net Delay	Logical Name (Net Name)
IBUF:I->O	2	1.106	0.532	B_IBUF (B_IBUF)
LUT3:I0->O	1	0.612	0.357	Cout1 (Cout_OBUF)
OBUF:I->O		3.169		Cout_OBUF (Cout)
Total		5.776ns		

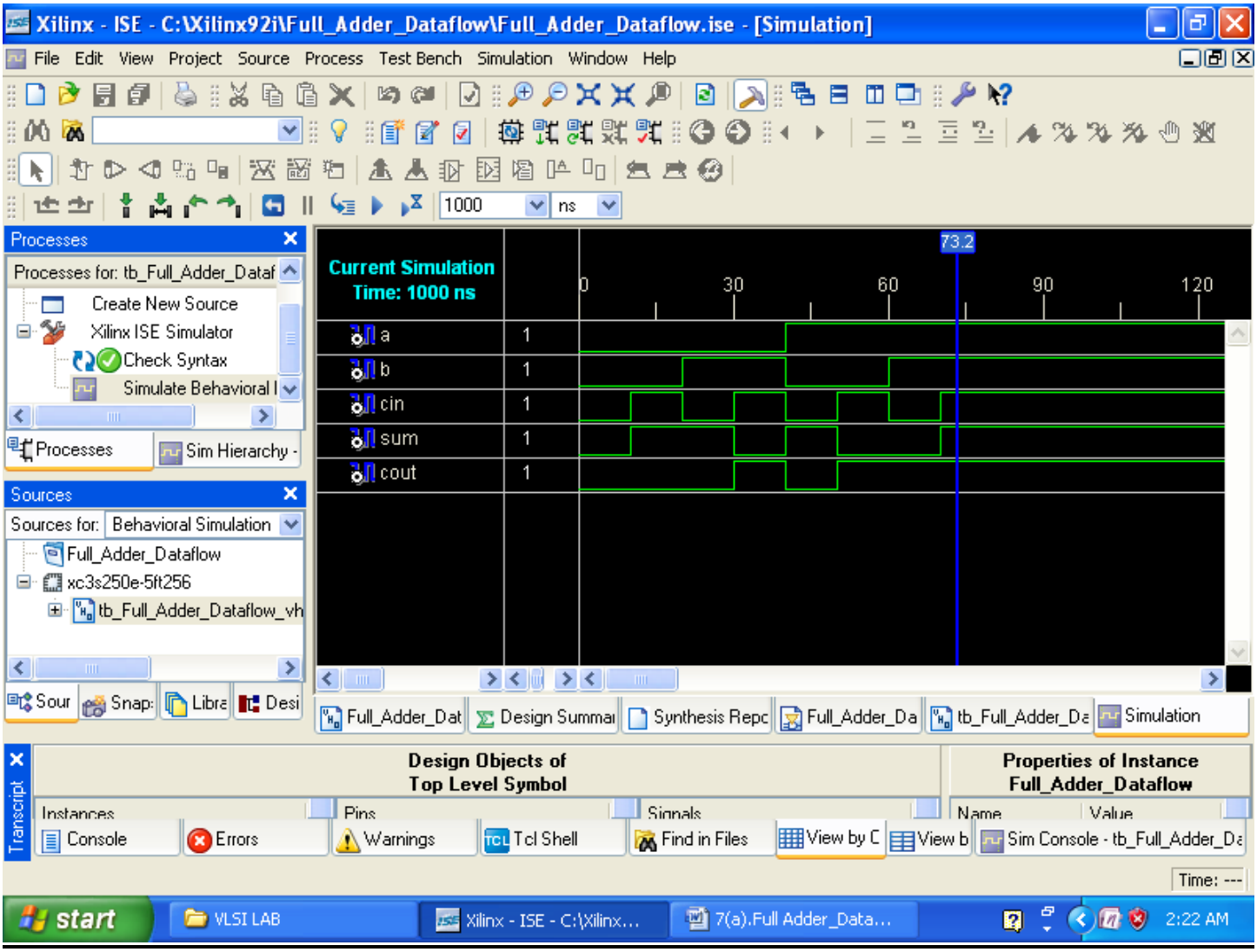
VHDL Test bench:

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.std_logic_unsigned.all;
USE ieee.numeric_std.ALL;
ENTITY tb_Full_Adder_Dataflow_vhd IS
END tb_Full_Adder_Dataflow_vhd;
ARCHITECTURE behavior OF tb_Full_Adder_Dataflow_vhd IS
        COMPONENT Full_Adder_Dataflow
    PORT(
        A : IN std_logic;
        B : IN std_logic;
```

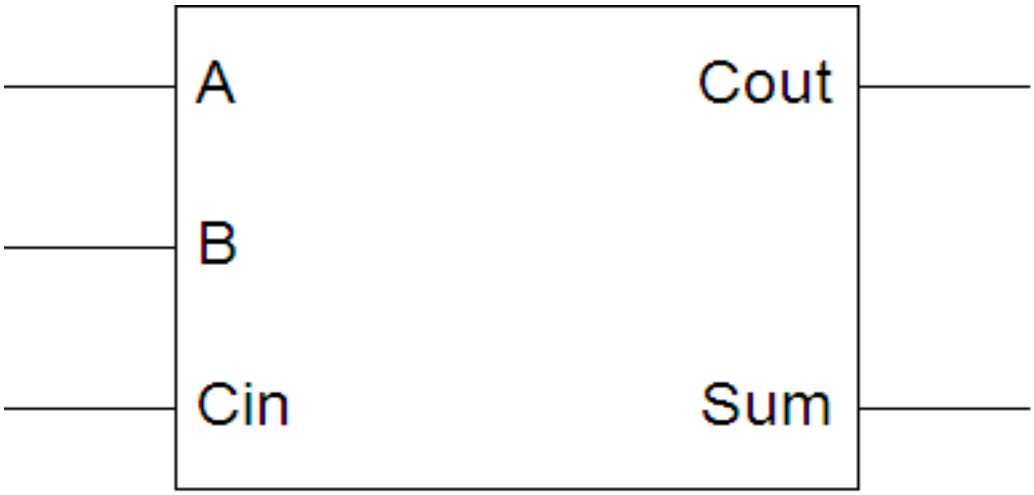
```
                Cin : IN std_logic;
                Sum : OUT std_logic;
                Cout : OUT std_logic
                );
        END COMPONENT;
        SIGNAL A :  std_logic := '0';
        SIGNAL B :  std_logic := '0';
        SIGNAL Cin :  std_logic := '0';
        SIGNAL Sum :  std_logic;
        SIGNAL Cout :  std_logic;
BEGIN
                uut: Full_Adder_Dataflow PORT MAP(
                A => A,
                B => B,
                Cin => Cin,
                Sum => Sum,
                Cout => Cout
        );
A<='1' after 40ns;
B<='1' after 20ns,'0' after 40ns,'1'after 60ns;
Cin<='1' after 10ns,'0' after 20ns,'1' after 30ns,'0' after 40ns,'1' after 50ns, '0' after 60ns,'1' after 70ns;
```

Result: Full Adder Using Dataflow Style is designed using VHDL and simulated the same using Xilinx ISE Simulator

Simulation Results:


Xilinx - ISE - C:\Xilinx92i\Full_Adder_Dataflow\Full_Adder_Dataflow.ise - [Simulation]
File Edit View Project Source Process Test Bench Simulation Window Help
1000 ns
Processes
Processes for: tb_Full_Adder_Dataf
Create New Source
Xilinx ISE Simulator
Check Syntax
Simulate Behavioral I
Processes
Sim Hierarchy -
Sources
Sources for: Behavioral Simulation
Full_Adder_Dataflow
xc3s250e-5ft256
tb_Full_Adder_Dataflow_vh
Current Simulation Time: 1000 ns
73.2
0
30
60
90
120
a
b
cin
sum
cout
1
Full_Adder_Dat
Design Summai
Synthesis Repc
Full_Adder_Da
tb_Full_Adder_Da
Simulation
Design Objects of Top Level Symbol
Properties of Instance Full_Adder_Dataflow
Instances
Pins
Signals
Name
Value
Transcript
Console
Errors
Warnings
Tcl Shell
Find in Files
View by C
View b
Sim Console - tb_Full_Adder_Da
Time: ---
start
VLSI LAB
Xilinx - ISE - C:\Xilinx...
7(a).Full Adder_Data...
2:22 AM

Schematic Diagram:



Experiment No:6 Full Adder Using Behavioral Style

Aim: To Design **Full Adder Using Behavioral Style** using VHDL and simulate the same using Xilinx ISE Simulator

Tools Required: 1.PC

2. Xilinx ISE

VHDL Code:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
entity Full_Adder_Behavioral is
   Port ( A : in  STD_LOGIC;
          B : in  STD_LOGIC;
          Cin : in  STD_LOGIC;
          Sum : out  STD_LOGIC;
          Cout : out  STD_LOGIC);
end Full_Adder_Behavioral;
architecture Behavioral of Full_Adder_Behavioral is
signal P:Std_logic_vector(2 downto 0);
   begin
    P<=A&B&Cin;
    process(A,B,p,Cin)
      begin
        case p is
            when "000"=>Sum<='0';Cout<='0';
            when "001"=>Sum<='1';Cout<='0';
            when "010"=>Sum<='1';Cout<='0';
            when "011"=>Sum<='0';Cout<='1';
            when "100"=>Sum<='1';Cout<='0';
            when "101"=>Sum<='0';Cout<='1';
            when "110"=>Sum<='0';Cout<='1';
            when "111"=>Sum<='1';Cout<='1';
```

```
            when others=>Sum<='Z';Cout<='Z';
          end case;
       end process;
    end Behavioral;
```

Synthesis Report

HDL Synthesis Report

Macro Statistics
ROMs : 1
8x2-bit ROM : 1

Final Report:

Final Results

RTL Top Level Output File Name : Full_Adder_Behavioral.ngr

Top Level Output File Name : Full_Adder_Behavioral

Output Format : NGC

Optimization Goal : Speed

Keep Hierarchy : NO

Design Statistics

IOs : 5

Cell Usage :

BELS : 2

LUT3 : 2

IO Buffers : 5

IBUF : 3

OBUF : 2

Device utilization summary:

Selected Device : 3s250eft256-5

Number of Slices: 1 out of 2448 0%

Number of 4 input LUTs: 2 out of 4896 0%

Number of IOs: 5

Number of bonded IOBs: 5 out of 172 2%

TIMING REPORT:

Delay: 5.776ns (Levels of Logic = 3)

Source: B (PAD)

Destination: Cout (PAD)

Data Path: B to Cout

Cell:in->out	fanout	Gate Delay	Net Delay	Logical Name (Net Name)
IBUF:I->O	2	1.106	0.532	B_IBUF (B_IBUF)
LUT3:I0->O	1	0.612	0.357	Mrom_P_rom000011 (Mrom_P_rom0000)
OBUF:I->O		3.169		Cout_OBUF (Cout)
Total		5.776ns		

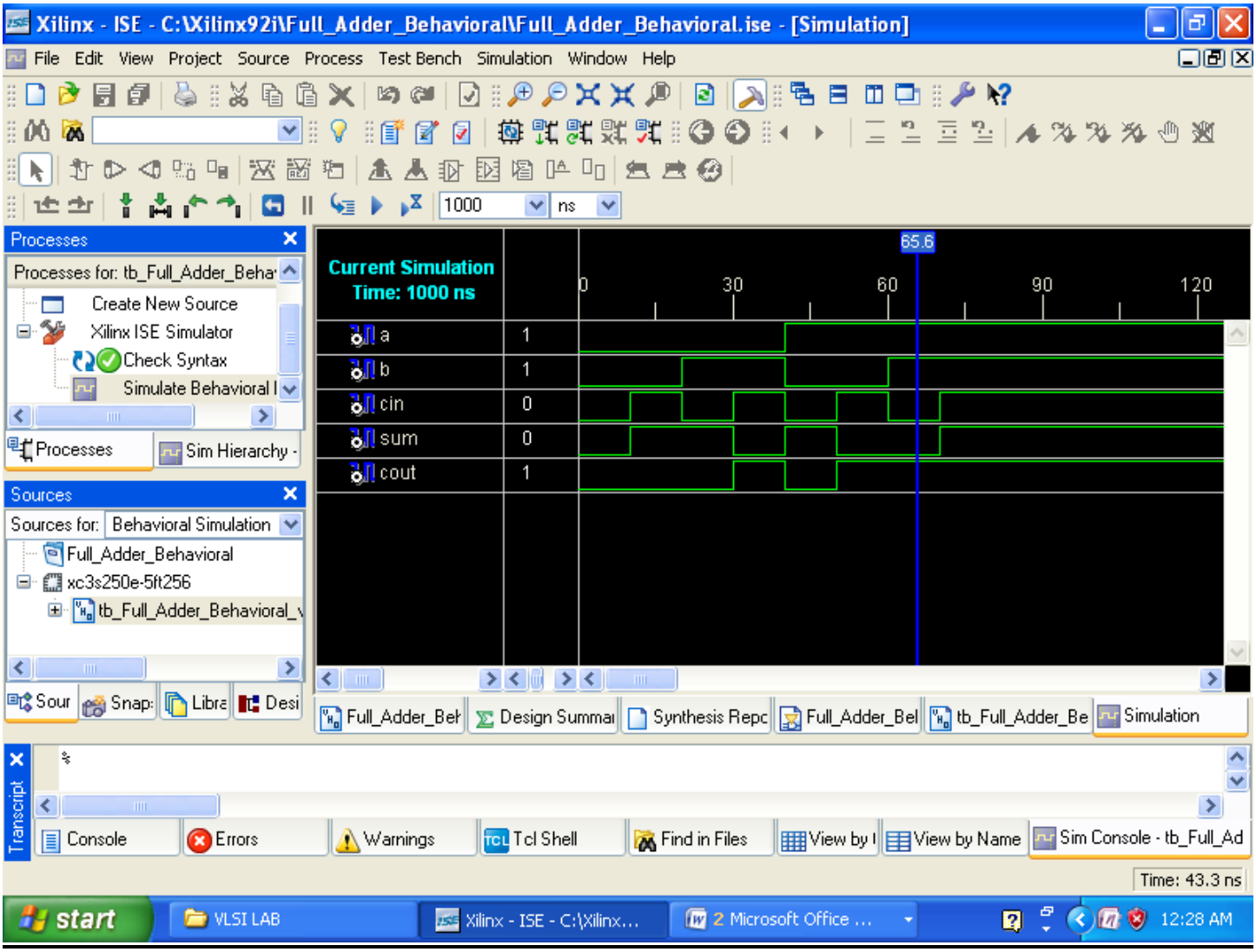
VHDL Test bench:

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.std_logic_unsigned.all;
USE ieee.numeric_std.ALL;
ENTITY tb_Full_Adder_Behavioral_vhd IS
END tb_Full_Adder_Behavioral_vhd;
ARCHITECTURE behavior OF tb_Full_Adder_Behavioral_vhd IS
        COMPONENT Full_Adder_Behavioral
    PORT(
        A : IN std_logic;
        B : IN std_logic;
        Cin : IN std_logic;
        Sum : OUT std_logic;
        Cout : OUT std_logic
        );
    END COMPONENT;
    SIGNAL A :  std_logic := '0';
    SIGNAL B :  std_logic := '0';
    SIGNAL Cin :  std_logic := '0';
    SIGNAL Sum :  std_logic;
    SIGNAL Cout :  std_logic;
BEGIN
        uut: Full_Adder_Behavioral PORT MAP(
        A => A,
        B => B,
        Cin => Cin,
```

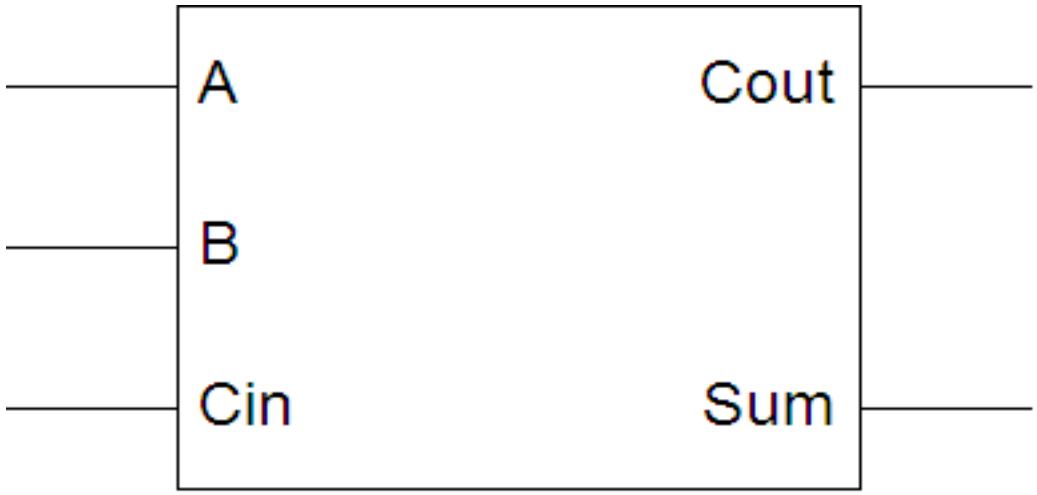
```
                Sum => Sum,
                Cout => Cout
        );
    A<='1' after 40ns;
    B<='1' after 20ns,'0' after 40ns,'1'after 60ns;
    Cin<='1' after 10ns,'0' after 20ns,'1' after 30ns,'0' after 40ns,'1' after 50ns, '0' after 60ns,'1' after 70ns;
```

Result: Full Adder Using Behavioral Style is designed using VHDL and simulated the same using Xilinx ISE Simulator

Simulation Results:



Schematic Diagram:



Experiment No:7 Full Adder Using Structural Style

Aim: To Design **Full Adder Using Structural Style** using VHDL and simulate the same using Xilinx ISE Simulator

Tools Required: 1.PC

2. Xilinx ISE

VHDL Code:

-------VHDL Code for Xor Gate----

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity or_gate is
   Port ( a : in  STD_LOGIC;
          b : in  STD_LOGIC;
          c : out  STD_LOGIC);
end or_gate;
architecture Behavioral of or_gate is
  begin
   c<=a or b;
end Behavioral;
```

-------VHDL Code for and Gate----

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity and_g is
   Port ( a : in  STD_LOGIC;
          b : in  STD_LOGIC;
          c : out  STD_LOGIC);
end and_g;
architecture Behavioral of and_g is
begin
c<=a and b;
end Behavioral;
```

-------VHDL Code for Or Gate----

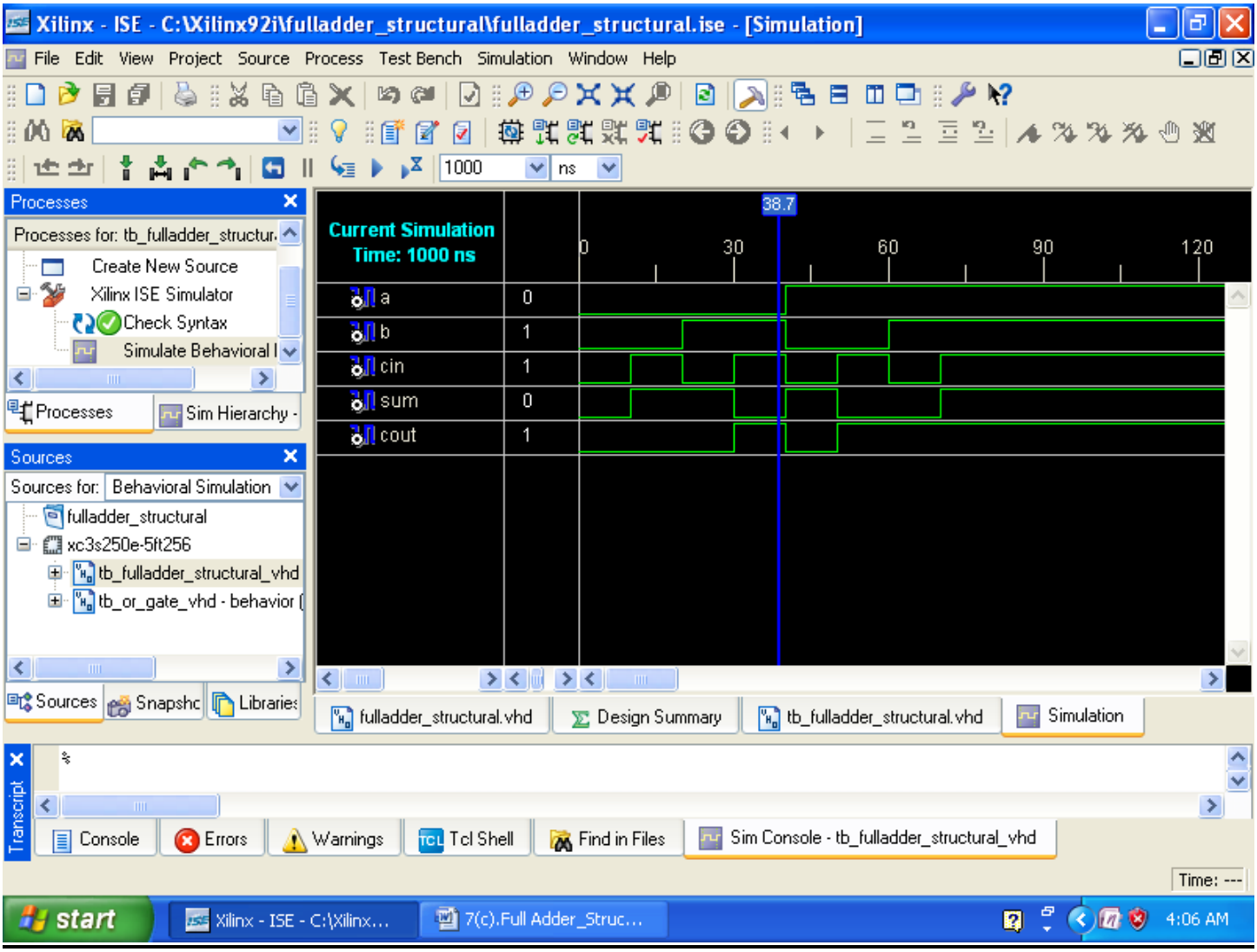
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity xor_g is
   Port ( a : in  STD_LOGIC;
          b : in  STD_LOGIC;
          c : out  STD_LOGIC);
end xor_g;


architecture Behavioral of xor_g is
begin
c<=a xor b;
end Behavioral;
```

-------VHDL Code for Full Adder----

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity fulladder_structural is
   Port ( A : in  STD_LOGIC;
          B : in  STD_LOGIC;
          Cin : in  STD_LOGIC;
          SUM : out  STD_LOGIC;
          Cout : out  STD_LOGIC);
end fulladder_structural;
architecture Behavioral of fulladder_structural is
 component or_gate is
```

```
        port(a,b:in std_logic;
             c:out std_logic);
   end component;
  component and_g is
        port(a,b:in std_logic;
             c:out std_logic);
end component;
component xor_g is
        port(a,b:in std_logic;
             c:out std_logic);
end component;
        signal y1,y2,y3:std_logic;
begin
x1:xor_g port map(A,B,y1);
a1:and_g port map(A,B,y2);
x2:xor_g port map(y1,Cin,sum);
a2:and_g port map(y1,Cin,y3);
r1:or_gate port map(y2,y3,Cout);
end Behavioral;
```

Simulation Results:

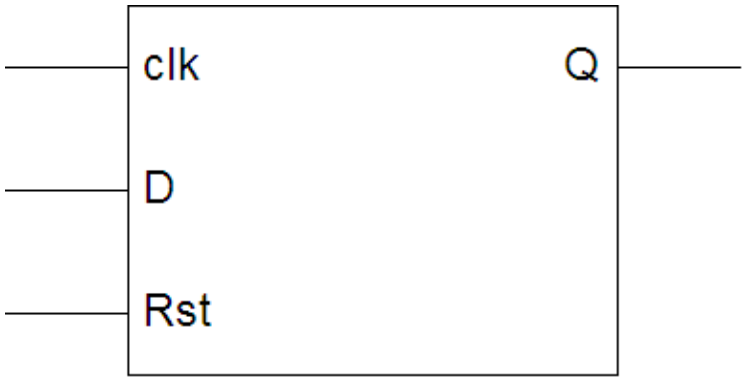

Xilinx - ISE - C:\Xilinx92i\fulladder_structural\fulladder_structural.ise - [Simulation]
File Edit View Project Source Process Test Bench Simulation Window Help
1000 ns
Processes
Processes for: tb_fulladder_structur
Create New Source
Xilinx ISE Simulator
Check Syntax
Simulate Behavioral I
Processes
Sim Hierarchy -
Sources
Sources for: Behavioral Simulation
fulladder_structural
xc3s250e-5ft256
tb_fulladder_structural_vhd
tb_or_gate_vhd - behavior
Sources
Snapshc
Libraries
Current Simulation Time: 1000 ns
38.7
0
30
60
90
120
a
b
cin
sum
cout
0
1
1
0
1
fulladder_structural.vhd
Design Summary
tb_fulladder_structural.vhd
Simulation
Transcript
Console
Errors
Warnings
Tcl Shell
Find in Files
Sim Console - tb_fulladder_structural_vhd
Time: ---
start
Xilinx - ISE - C:\Xilinx...
7(c).Full Adder_Struc...
4:06 AM

VHDL Test bench:

```
ENTITY tb_fulladder_structural_vhd IS
END tb_fulladder_structural_vhd;
ARCHITECTURE behavior OF tb_fulladder_structural_vhd IS
        COMPONENT fulladder_structural
        PORT(
                A : IN std_logic;
                B : IN std_logic;
                Cin : IN std_logic;
                SUM : OUT std_logic;
                Cout : OUT std_logic
                );
        END COMPONENT;
        SIGNAL A :  std_logic := '0';
        SIGNAL B :  std_logic := '0';
        SIGNAL Cin :  std_logic := '0';
        SIGNAL SUM :  std_logic;
        SIGNAL Cout :  std_logic;

BEGIN
        uut: fulladder_structural PORT MAP(
                A => A,
                B => B,
                Cin => Cin,
                SUM => SUM,
                Cout => Cout
        );

A<='1' after 40ns;
B<='1' after 20ns,'0' after 40ns,'1'after 60ns;
Cin<='1' after 10ns,'0' after 20ns,'1' after 30ns,'0' after 40ns,'1' after 50ns, '0' after 60ns,'1' after 70ns;
END;
```

Result: Full Adder Using Structural Style is designed using VHDL and simulated the same using Xilinx ISE Simulator

Schematic Diagram:



Synthesis Report

HDL Synthesis Report

Macro Statistics

Registers : 1

1-bit register : 1

Advanced HDL Synthesis Report

Macro Statistics

Registers : 1

Flip-Flops : 1

Final Register Report

Macro Statistics

Registers : 1

Flip-Flops : 1

Final Report:

Final Results

RTL Top Level Output File Name : DFF_Asyn.ngr

Top Level Output File Name : DFF_Asyn

Output Format : NGC

Optimization Goal : Speed

Keep Hierarchy : NO

Experiment No:8 8-To-3 Encoder with Priority

Aim: To Design **8-To-3 Encoder with Priority** using VHDL and simulate the same using Xilinx ISE Simulator.

Tools Required: 1.PC

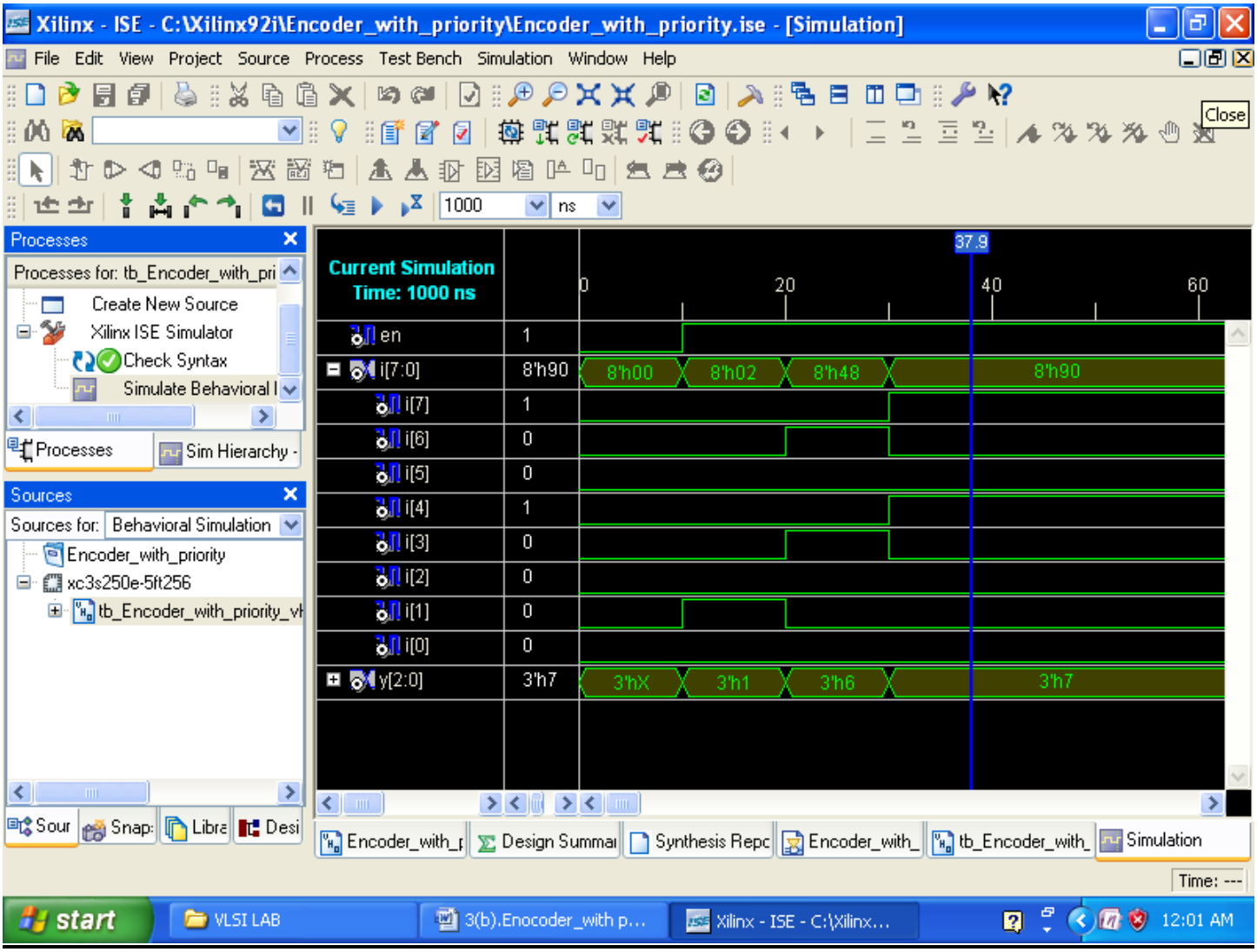
2. Xilinx ISE

VHDL Code:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
entity Encoder_with_priority is
   Port ( En : in  STD_LOGIC;
          I : in  STD_LOGIC_VECTOR (7 downto 0);
          Y : out  STD_LOGIC_VECTOR (2 downto 0));
end Encoder_with_priority;
architecture Behavioral of Encoder_with_priority is
begin
process(En,I)
begin
  if En='0'  then Y<="XXX";
  elsif I(7)='1' then Y<="111";
  elsif I(6)='1' then Y<="110";
  elsif I(5)='1' then Y<="101";
  elsif I(4)='1' then Y<="100";
  elsif I(3)='1' then Y<="011";
  elsif I(2)='1' then Y<="010";
```

```
    elsif I(1)='1' then Y<="001";
    elseif I(0)='1' thenY<="000";
  else Y<="ZZZ";
   end if;
  end process;
  end Behavioral;
```

Simulation Results:



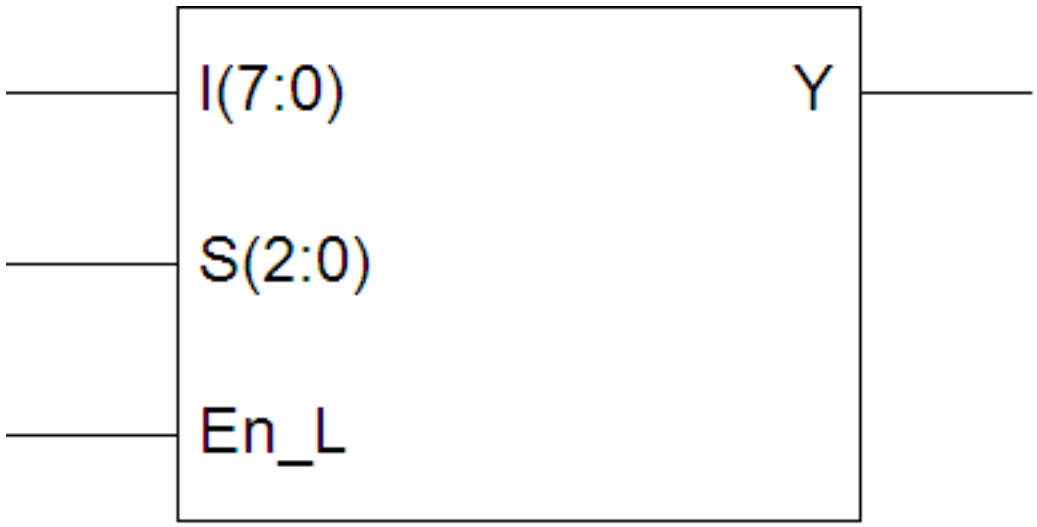
VHDL Test bench:

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.std_logic_unsigned.all;
USE ieee.numeric_std.ALL;
ENTITY tb_encoder_with_priority_vhd IS
END tb_encoder_with_priority_vhd;
ARCHITECTURE behavior OF tb_encoder_with_priority_vhd IS
        COMPONENT encoder_with_priority
    PORT(
        En : IN std_logic;
        I : IN std_logic_vector(7 downto 0);
        Y : OUT std_logic_vector(2 downto 0)
        );
    END COMPONENT;
    SIGNAL En :  std_logic := '0';
    SIGNAL I :  std_logic_vector(7 downto 0) := (others=>'0');
    SIGNAL Y :  std_logic_vector(2 downto 0);
BEGIN
```

```
        uut: encoder_with_priority PORT MAP(
                En => En,
                I => I,
                Y => Y
        );
    En<='1' after 10ns;
    I<="00000010" after 10ns,"00001000" after 20ns,"01000000" after 30ns;
```

Result: 8-To-3 Encoder with Priority is designed using VHDL and simulated the same using Xilinx ISE Simulator

Schematic Diagram:



Experiment No:9 Binary-To-Gray Code Converter

Aim: To Design **Binary-To-Gray Code Converter** using VHDL and simulate the same using Xilinx ISE Simulator

Tools Required: 1.PC

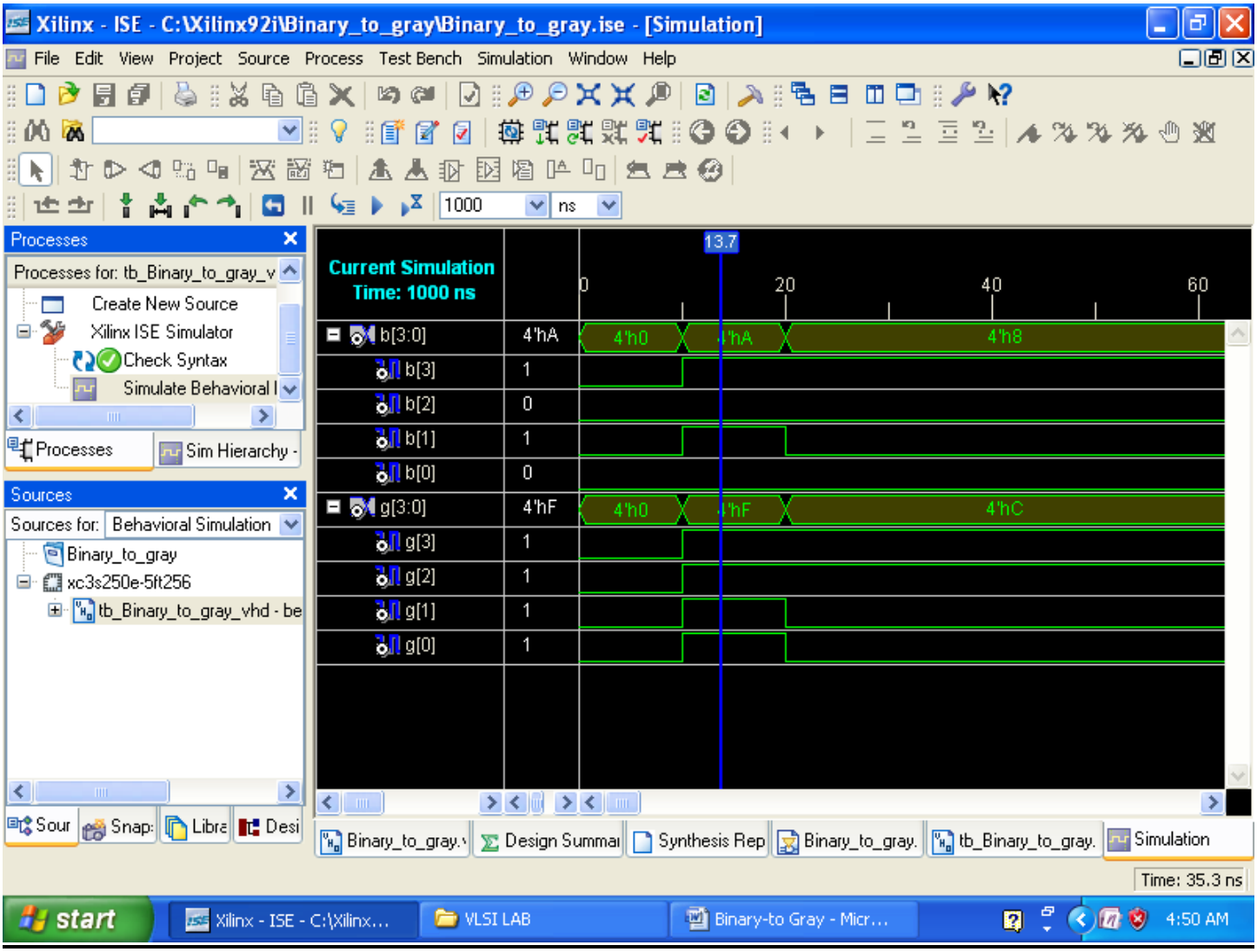
2. Xilinx ISE

VHDL Code:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
entity Binary_to_gray is
   Port ( B : in  STD_LOGIC_VECTOR (3 downto 0);
          G : out  STD_LOGIC_VECTOR (3 downto 0));
end Binary_to_gray;
```

```
architecture Behavioral of Binary_to_gray is
begin
G(3)<=B(3);
G(2)<=B(3) XOR B(2);
G(1)<=B(2) XOR B(1);
G(0)<=B(1) XOR B(0);
end Behavioral;
```

Simulation Results:

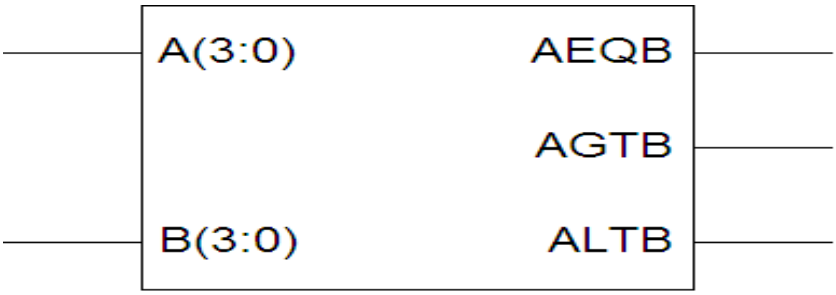

Xilinx - ISE - C:\Xilinx92i\Binary_to_gray\Binary_to_gray.ise - [Simulation]
File Edit View Project Source Process Test Bench Simulation Window Help
1000 ns
Processes
Processes for: tb_Binary_to_gray_v
Create New Source
Xilinx ISE Simulator
Check Syntax
Simulate Behavioral I
Processes
Sim Hierarchy -
Sources
Sources for: Behavioral Simulation
Binary_to_gray
xc3s250e-5ft256
tb_Binary_to_gray_vhd - be
Sour
Snap
Libra
Desi
Current Simulation Time: 1000 ns
13.7
0
20
40
60
b[3:0] 4'hA 4'h0 4'hA 4'h8
b[3] 1
b[2] 0
b[1] 1
b[0] 0
g[3:0] 4'hF 4'h0 4'hF 4'hC
g[3] 1
g[2] 1
g[1] 1
g[0] 1
Binary_to_gray.
Design Summar
Synthesis Rep
Binary_to_gray.
tb_Binary_to_gray.
Simulation
Time: 35.3 ns
start
Xilinx - ISE - C:\Xilinx...
VLSI LAB
Binary-to Gray - Micr...
4:50 AM

VHDL Test bench:

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.std_logic_unsigned.all;
USE ieee.numeric_std.ALL;
ENTITY tb_Binary_to_gray_vhd IS
END tb_Binary_to_gray_vhd;
ARCHITECTURE behavior OF tb_Binary_to_gray_vhd IS
        COMPONENT Binary_to_gray
    PORT(
        B : IN std_logic_vector(3 downto 0);
        G : OUT std_logic_vector(3 downto 0)
        );
    END COMPONENT;
    SIGNAL B :  std_logic_vector(3 downto 0) := (others=>'0');
    SIGNAL G :  std_logic_vector(3 downto 0);

BEGIN
        uut: Binary_to_gray PORT MAP(
        B => B,
        G => G
    );
    B<="1010" after 10ns,"1000" after 20ns;

END;
```

Result: Binary-To-Gray Code Converter is designed using VHDL and simulated the same using Xilinx ISE Simulator

Schematic Diagram:



Synthesis Report

HDL Synthesis Report

Macro Statistics
Comparators : 2
4-bit comparator equal : 1
4-bit comparator greater : 1

Final Report:

RTL Top Level Output File Name : comparator.ngr
Top Level Output File Name : comparator
Output Format : NGC
Optimization Goal : Speed
Keep Hierarchy : NO

Design Statistics

IOs : 11

Cell Usage :

BELS : 12
LUT4 : 9
MUXF5 : 3
IO Buffers : 11
IBUF : 8
OBUF : 3

Device utilization summary:

Selected Device: 3s250eft256-5
Number of Slices: 5 out of 2448 0%
Number of 4 input LUTs: 9 out of 4896 0%
Number of IOs: 11
Number of bonded IOBs: 11 out of 172 6%

TIMING REPORT:

Data Path: B<1> to AGTB

Cell:in->out	fanout	Gate Delay	Net Delay	Logical Name (Net Name)

IBUF:I->O	3	1.106	0.603	B_1_IBUF (B_1_IBUF)
LUT4:I0->O	2	0.612	0.532	AGTB31 (AGTB_bdd2)
LUT4:I0->O	1	0.612	0.000	AGTB111 (N14)
MUXF5:I1->O	1	0.278	0.357	AGTB11_f5 (AGTB_OBUF)
OBUF:I->O		3.169		AGTB_OBUF (AGTB)

Total 7.269ns

Experiment No:10 D Flip Flop with Asynchronous "Reset"

Aim: To Design **D Flip Flop with Asynchronous "Reset"** using VHDL and simulate the same using Xilinx ISE Simulator

Tools Required: 1.PC

2. Xilinx ISE

VHDL Code:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
entity DFF_Asyn is
   Port ( clk : in  STD_LOGIC;
          Rst : in  STD_LOGIC;
          D : in  STD_LOGIC;
          Q : out  STD_LOGIC);
end DFF_Asyn;
architecture Behavioral of DFF_Asyn is
begin
    process(clk,D,Rst)
    begin
         if Rst='1' then Q<='0';
        elsif clk'event and clk='1' then
        Q<=D;
       end if;
      end process;
end Behavioral;
```

Design Statistics

IOs : 4

Cell Usage :

FlipFlops/Latches : 1

FDC : 1

Clock Buffers : 1

BUFGP : 1

IO Buffers : 3

IBUF : 2

OBUF : 1

==========

Device utilization summary:

Selected Device : 3s250eft256-5

Number of Slices:	0	out of 2448	0%
Number of Slice Flip Flops:	1	out of 4896	0%
Number of IOs:	4		
Number of bonded IOBs:	4	out of 172	2%
IOB Flip Flops:	1		
Number of GCLKs:	1	out of 24	4%

TIMING REPORT:

Clock Information:

Clock Signal	Clock buffer(FF name)	Load
clk	BUFGP	1

Asynchronous Control Signals Information:

Control Signal	Buffer(FF name)	Load
Rst	IBUF	1

Timing Summary:

Speed Grade: -5

Minimum period: No path found

Minimum input arrival time before clock: 1.731ns

Maximum output required time after clock: 4.040ns

Maximum combinational path delay: No path found

Timing Detail:

All values displayed in nanoseconds (ns)

==========

Timing constraint: Default OFFSET IN BEFORE for Clock 'clk'

Total number of paths / destination ports: 1 / 1

Offset: 1.731ns (Levels of Logic = 1)

Source: D (PAD)

Destination: Q (FF)

Destination Clock: clk rising

Data Path: D to Q

Cell:in->out	fanout	Gate Delay	Net Delay	Logical Name (Net Name)
IBUF:I->O	1	1.106	0.357	D_IBUF (D_IBUF)
FDC:D		0.268		Q
Total		1.731ns (1.374ns logic, 0.357ns route)		

==========

Timing constraint: Default OFFSET OUT AFTER for Clock 'clk'

Total number of paths / destination ports: 1 / 1

Offset: 4.040ns (Levels of Logic = 1)

Source: Q (FF)

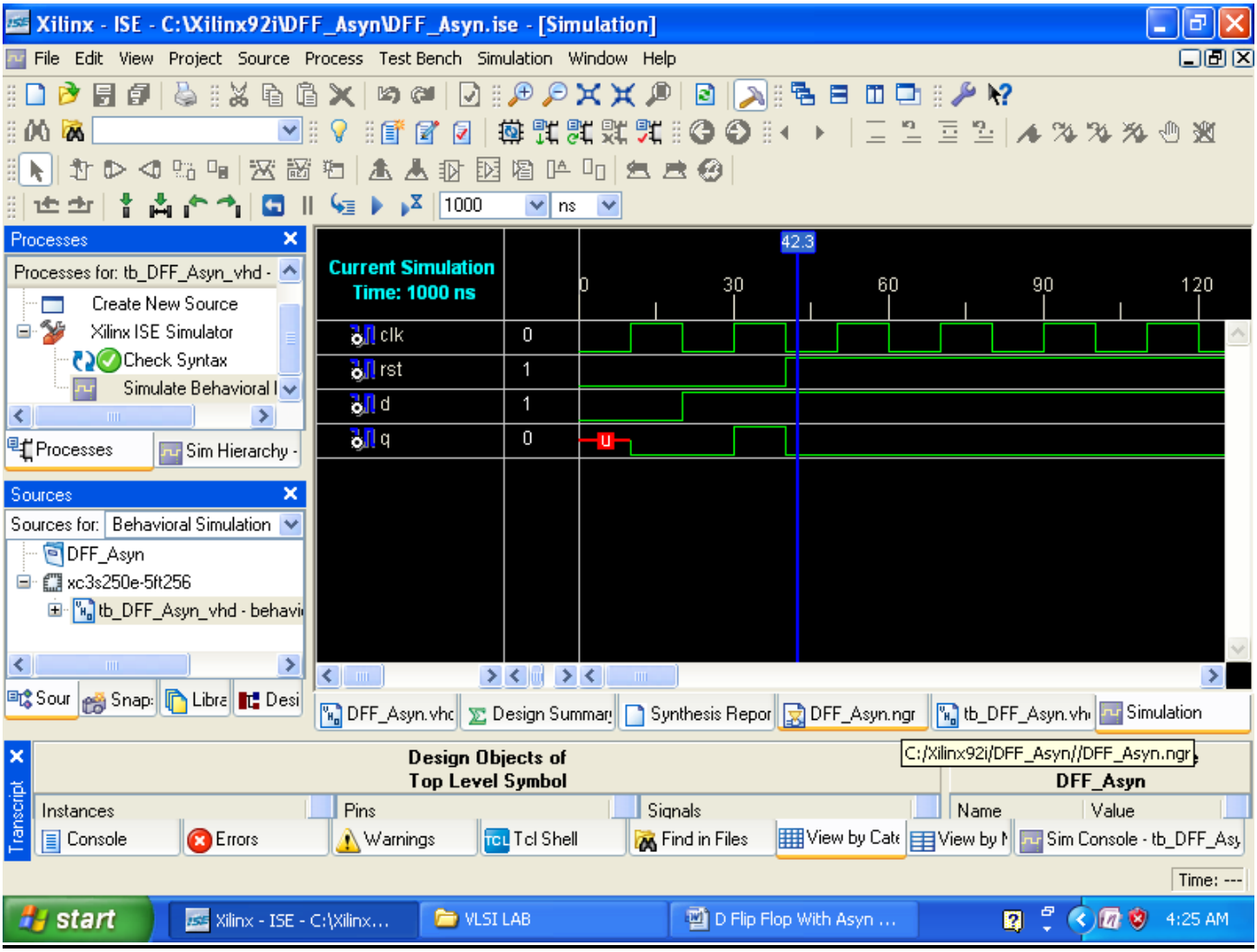
Destination: Q (PAD)

Source Clock: clk rising

Data Path: Q to Q:

Cell:in->out	fanout	Gate Delay	Net Delay	Logical Name (Net Name)
FDC:C->Q	1	0.514	0.357	Q (Q_OBUF)
OBUF:I->O		3.169		Q_OBUF (Q)
Total		4.040ns		

Simulation Results:


Xilinx - ISE - C:\Xilinx92i\DFF_Asyn\DFF_Asyn.ise - [Simulation]
File Edit View Project Source Process Test Bench Simulation Window Help
1000 ns
Processes
Processes for: tb_DFF_Asyn_vhd -
Create New Source
Xilinx ISE Simulator
Check Syntax
Simulate Behavioral I
Processes
Sim Hierarchy -
Sources
Sources for: Behavioral Simulation
DFF_Asyn
xc3s250e-5ft256
tb_DFF_Asyn_vhd - behavi
Current Simulation Time: 1000 ns
42.3
0
30
60
90
120
clk
rst
d
q
DFF_Asyn.vhd
Design Summar
Synthesis Repor
DFF_Asyn.ngr
tb_DFF_Asyn.vh
Simulation
Design Objects of Top Level Symbol
C:/Xilinx92i/DFF_Asyn/DFF_Asyn.ngr
DFF_Asyn
Instances
Pins
Signals
Name
Value
Transcript
Console
Errors
Warnings
Tcl Shell
Find in Files
View by Cate
View by N
Sim Console - tb_DFF_Asy
Time: ---
start
Xilinx - ISE - C:\Xilinx...
VLSI LAB
D Flip Flop With Asyn ...
4:25 AM

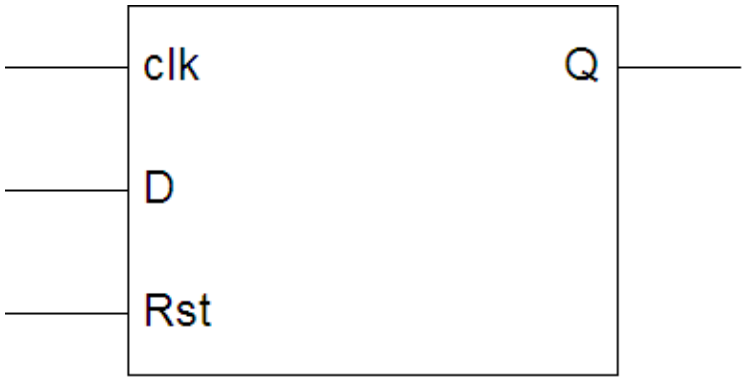
VHDL Test bench:

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.std_logic_unsigned.all;
USE ieee.numeric_std.ALL;
ENTITY tb_DFF_Asyn_vhd IS
END tb_DFF_Asyn_vhd;
ARCHITECTURE behavior OF tb_DFF_Asyn_vhd IS
        COMPONENT DFF_Asyn
        PORT(clk : IN std_logic;
                Rst : IN std_logic;
                D : IN std_logic;
                Q : OUT std_logic
                );
        END COMPONENT;
        SIGNAL clk :  std_logic := '0';
        SIGNAL Rst :  std_logic := '0';
        SIGNAL D :  std_logic := '0';
        SIGNAL Q :  std_logic;
BEGIN
        uut: DFF_Asyn PORT MAP(
                clk => clk,
                Rst => Rst,
                D => D,
                Q => Q  );
Rst<='1' after 40ns;
clk<= not clk after 10ns;
D<='1' after 20ns;
```

```
END;
```

Result: **D Flip Flop with Asynchronous "Reset"** is designed using VHDL and simulated the same using Xilinx ISE Simulator

Schematic Diagram:



Experiment No:11 D Flip Flop with Synchronous "Reset"

Aim: To Design **D Flip Flop with Synchronous "Reset"** using VHDL and simulate the same using Xilinx ISE Simulator

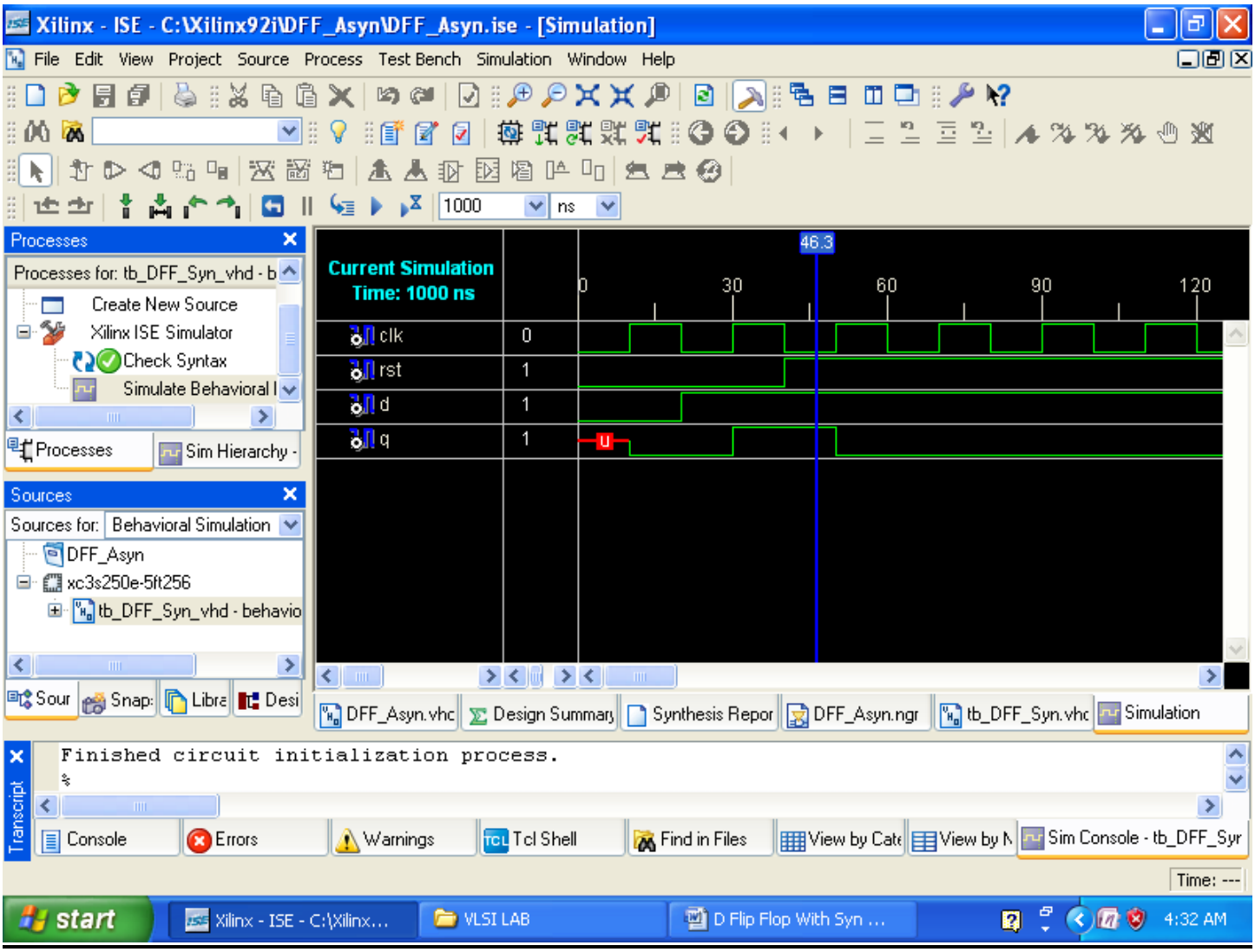
Tools Required: 1.PC

2. Xilinx ISE

VHDL Code:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
entity DFF_Syn is
   Port ( clk : in  STD_LOGIC;
          Rst : in  STD_LOGIC;
          D : in  STD_LOGIC;
          Q : out  STD_LOGIC);
end DFF_Syn;
architecture Behavioral of DFF_Syn is
begin
    process
    begin
wait until clk'event and clk='1';
          if Rst='1' then Q<='0';
         elsif clk'event and clk='1' then
         Q<=D;
        end if;
       end process;
end Behavioral;
```

Simulation Results:



VHDL Test bench:

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.std_logic_unsigned.all;
USE ieee.numeric_std.ALL;
ENTITY tb_DFF_Syn_vhd IS
END tb_DFF_Syn_vhd;
ARCHITECTURE behavior OF tb_DFF_Syn_vhd IS
        COMPONENT DFF_Syn
        PORT(clk : IN std_logic;
                Rst : IN std_logic;
                D : IN std_logic;
                Q : OUT std_logic
                );
        END COMPONENT;
        SIGNAL clk :  std_logic := '0';
        SIGNAL Rst :  std_logic := '0';
        SIGNAL D :  std_logic := '0';
```

```
        SIGNAL Q :  std_logic;
BEGIN
        uut: DFF_Syn PORT MAP(
                clk => clk,
                Rst => Rst,
                D => D,
                Q => Q  );
Rst<='1' after 40ns;
clk<= not clk after 10ns;
D<='1' after 20ns;
END;
```

Result: **D Flip Flop with Synchronous "Reset"** is designed using VHDL and simulated the same using Xilinx ISE Simulator

Schematic Diagram:

Synthesis Report

HDL Synthesis Report

Macro Statistics

Registers : 1

1-bit register : 1

Advanced HDL Synthesis Report

Macro Statistics

Registers : 1

Flip-Flops : 1

Final Register Report

Macro Statistics

Registers : 1

Flip-Flops : 1

Final Report:

Final Results

RTL Top Level Output File Name : DFF_Asyn.ngr

Top Level Output File Name : DFF_Asyn

Output Format : NGC

Optimization Goal : Speed

Keep Hierarchy : NO

Experiment No:12 T Flip Flop with Asynchronous "Reset"

Aim: To Design T **Flip Flop with Asynchronous "Reset"** using VHDL and simulate the same using Xilinx ISE Simulator

Tools Required: 1.PC

2. Xilinx ISE

VHDL Code:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
entity TFF_Asyn is
   Port ( Rst : in  STD_LOGIC;
          clk : in  STD_LOGIC;
          T : in  STD_LOGIC;
          Q : out  STD_LOGIC);
```

```
end TFF_Asyn;
architecture Behavioral of TFF_Asyn is
begin
   process(Rst,Clk,T)
   begin
       if Rst='1'  then Q<='0';
      elsif clk'event and Clk='1' then Q<=not T;
      end if;
 end process;
end Behavioral;
```

Design Statistics

```
# IOs                    : 4
Cell Usage :
# BELS                   : 1
#  INV                   : 1
# FlipFlops/Latches      : 1
# FDC                    : 1
# Clock Buffers          : 1
# BUFGP                  : 1
# IO Buffers             : 3
# IBUF                   : 2
#  OBUF                  :1
=========================================================================
```

Device utilization summary:

Selected Device : 3s250eft256-5

Number of Slices:	1	out of 2448	0%
Number of Slice Flip Flops:	1	out of 4896	0%
Number of IOs:	4		
Number of bonded IOBs:	4	out of 172	2%
IOB Flip Flops:	1		
Number of GCLKs:	1	out of 24	4%

TIMING REPORT:

Clock Information:

Clock Signal	Clock buffer(FF name)	Load
clk	BUFGP	1

Asynchronous Control Signals Information:

Control Signal	Buffer(FF name)	Load
Rst	IBUF	1

Timing Summary:
Speed Grade: -5
Minimum period: No path found
Minimum input arrival time before clock: 2.7004ns
Maximum output required time after clock: 4.040ns
Maximum combinational path delay: No path found

Timing Detail:

All values displayed in nanoseconds (ns)

==========

Timing constraint: Default OFFSET IN BEFORE for Clock 'clk'
Total number of paths / destination ports: 1 / 1

Offset: 2.700ns (Levels of Logic = 2)
Source: T (PAD)
Destination: Q (FF)
Destination Clock: clk rising

Data Path: T to Q

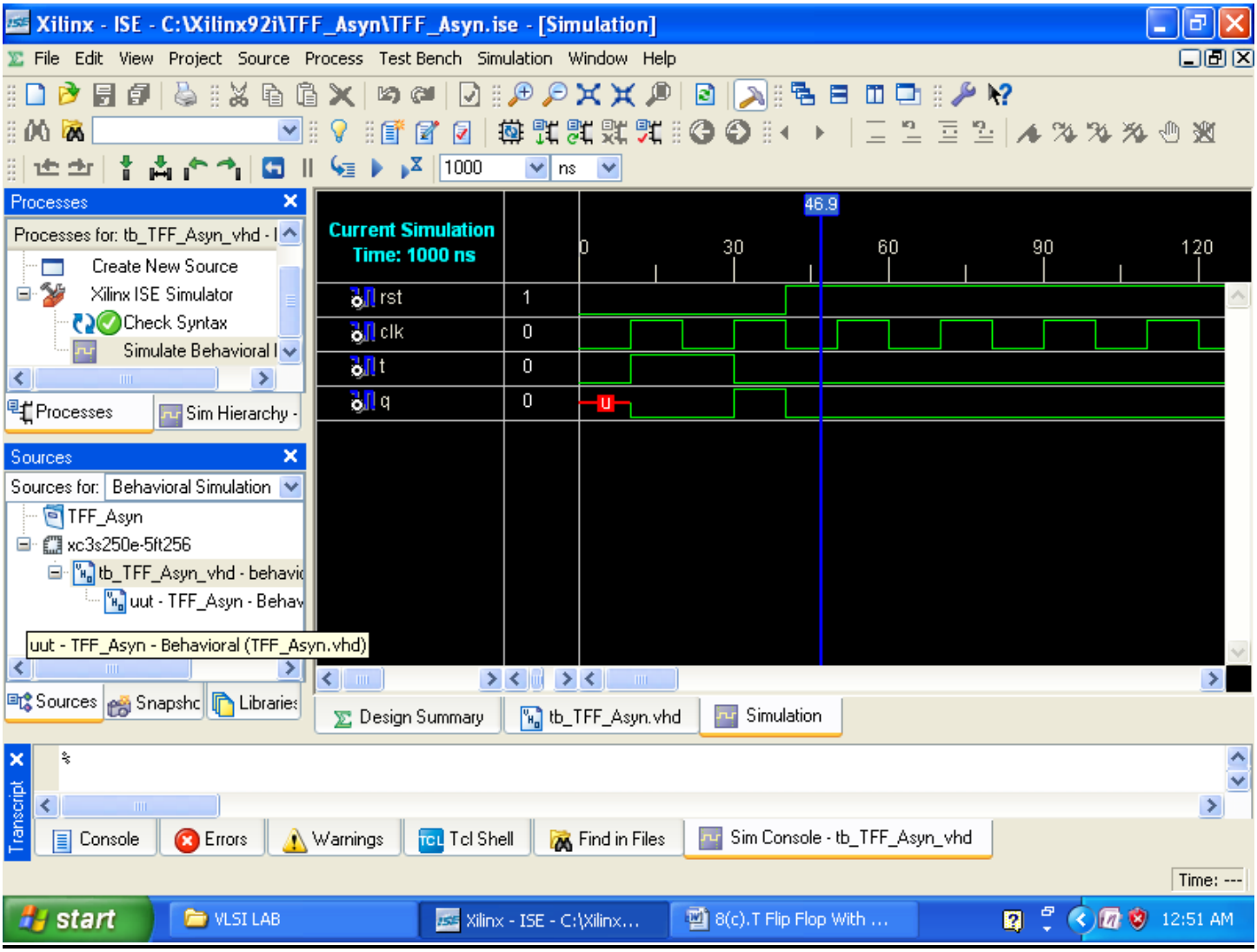
Gate Net

```
    Cell:in->out      fanout    Delay    Delay    Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O           1       1.106    0.357     T_IBUF (T_IBUF)
     INV:I->O            1       0.612    0.357     Q_not00011_INV_0 (Q_not0001)
     FDC:D                       0.268              Q
    ----------------------------------------
    Total                        2.700ns
   =========================================================================
    Timing constraint: Default OFFSET OUT AFTER for Clock 'clk'
    Total number of paths / destination ports: 1 / 1
  -------------------------------------------------------------------------
   Offset:            4.040ns (Levels of Logic = 1)
   Source:            Q (FF)
   Destination:       Q (PAD)
   Source Clock:      clk rising
```

Data Path: Q to Q

```
                                 Gate     Net
    Cell:in->out      fanout    Delay    Delay    Logical Name (Net Name)
    ----------------------------------------  ------------
     FDC:C->Q            1       0.514    0.357    Q (Q_OBUF)
     OBUF:I->O                   3.169             Q_OBUF (Q)
    ----------------------------------------
    Total                        4.040ns
   =========================================================================
```

Simulation Results:


Xilinx - ISE - C:\Xilinx92i\TFF_Asyn\TFF_Asyn.ise - [Simulation]
File Edit View Project Source Process Test Bench Simulation Window Help
1000 ns
Processes
Processes for: tb_TFF_Asyn_vhd - I
Create New Source
Xilinx ISE Simulator
Check Syntax
Simulate Behavioral I
Processes
Sim Hierarchy -
Sources
Sources for: Behavioral Simulation
TFF_Asyn
xc3s250e-5ft256
tb_TFF_Asyn_vhd - behavic
uut - TFF_Asyn - Behav
uut - TFF_Asyn - Behavioral (TFF_Asyn.vhd)
Sources
Snapshc
Libraries
Current Simulation Time: 1000 ns
46.9
0
30
60
90
120
rst
clk
t
q
1
0
0
U
Design Summary
tb_TFF_Asyn.vhd
Simulation
Transcript
Console
Errors
Warnings
Tcl Shell
Find in Files
Sim Console - tb_TFF_Asyn_vhd
Time: ---
start
VLSI LAB
Xilinx - ISE - C:\Xilinx...
8(c).T Flip Flop With ...
12:51 AM

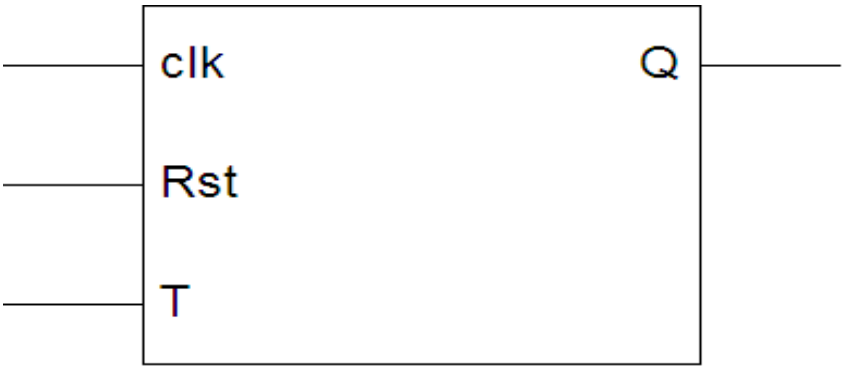
VHDL Test bench:

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.std_logic_unsigned.all;
USE ieee.numeric_std.ALL;
ENTITY tb_TFF_Asyn_vhd IS
END tb_TFF_Asyn_vhd;
ARCHITECTURE behavior OF tb_TFF_Asyn_vhd IS
        -- Component Declaration for the Unit Under Test (UUT)
        COMPONENT TFF_Asyn
        PORT(
                Rst : IN std_logic;
                clk : IN std_logic;
                T : IN std_logic;
                Q : OUT std_logic
                );
        END COMPONENT;
        SIGNAL Rst :  std_logic := '0';
        SIGNAL clk :  std_logic := '0';
        SIGNAL T :  std_logic := '0';
        SIGNAL Q :  std_logic;
BEGIN
        -- Instantiate the Unit Under Test (UUT)
        uut: TFF_Asyn PORT MAP(
                Rst => Rst,
                clk => clk,
                T => T,
                Q => Q
        );
        Clk<= not Clk after 10ns;
        Rst<='1' after 40ns;
```

```
T<='1' after 10ns,'0' after 30ns;
```

Result: **T Flip Flop with Asynchronous "Reset"** is designed using VHDL and simulated the same using Xilinx ISE Simulator.

Schematic Diagram:



Experiment No:13 T Flip Flop with Synchronous "Reset"

Aim: To Design **T Flip Flop with Synchronous "Reset"** using VHDL and simulate the same using Xilinx ISE Simulator

Tools Required: 1.PC

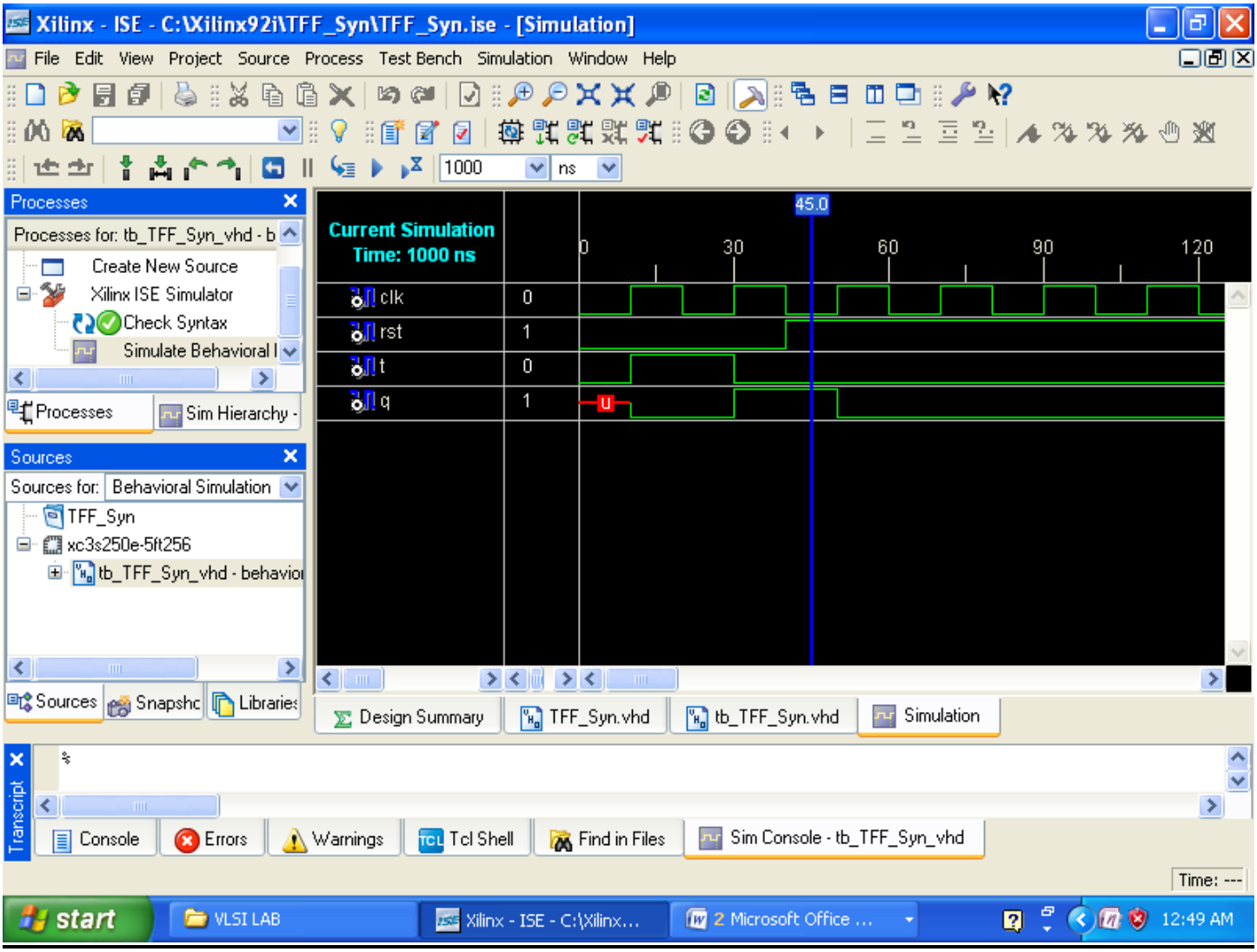
2. Xilinx ISE

VHDL Code:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
entity TFF_Syn is
   Port ( Clk : in  STD_LOGIC;
          Rst : in  STD_LOGIC;
          T : in  STD_LOGIC;
          Q : out  STD_LOGIC);
end TFF_Syn;
architecture Behavioral of TFF_Syn is
begin
  process
  begin
    wait until clk'event and clk='1';
```

```
    if Rst='1' then Q<='0';
    elsif Clk'event and clk='1' then Q<= not T;
   end if;
  end process;
end Behavioral;
```

Simulation Results:


Xilinx - ISE - C:\Xilinx92i\TFF_Syn\TFF_Syn.ise - [Simulation]
File Edit View Project Source Process Test Bench Simulation Window Help
1000 ns
Processes
Processes for: tb_TFF_Syn_vhd - b
Create New Source
Xilinx ISE Simulator
Check Syntax
Simulate Behavioral I
Processes
Sim Hierarchy -
Sources
Sources for: Behavioral Simulation
TFF_Syn
xc3s250e-5ft256
tb_TFF_Syn_vhd - behavio
Sources
Snapshc
Librarie
Current Simulation Time: 1000 ns
45.0
0
30
60
90
120
clk 0
rst 1
t 0
q 1
U
Design Summary
TFF_Syn.vhd
tb_TFF_Syn.vhd
Simulation
Transcript
Console
Errors
Warnings
Tcl Shell
Find in Files
Sim Console - tb_TFF_Syn_vhd
Time: ---
start
VLSI LAB
Xilinx - ISE - C:\Xilinx...
2 Microsoft Office ...
12:49 AM

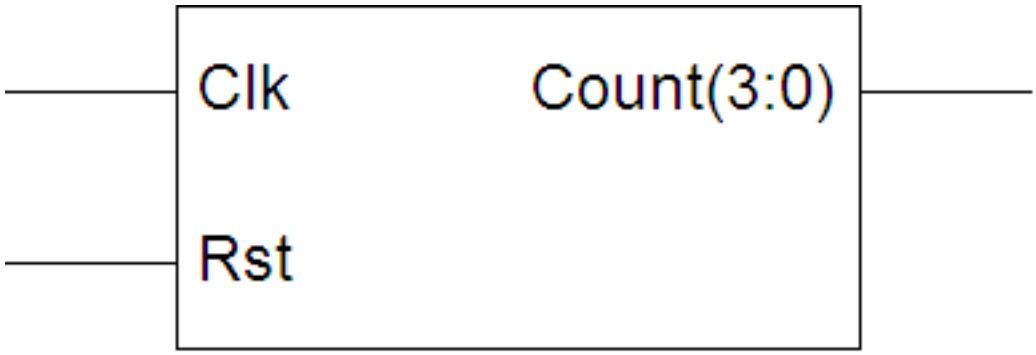
VHDL Test bench:

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.std_logic_unsigned.all;
USE ieee.numeric_std.ALL;
ENTITY tb_TFF_Syn_vhd IS
END tb_TFF_Syn_vhd;
ARCHITECTURE behavior OF tb_TFF_Syn_vhd IS
        COMPONENT TFF_Syn
        PORT(
                Clk : IN std_logic;
                Rst : IN std_logic;
                T : IN std_logic;
                Q : OUT std_logic
                );
        END COMPONENT;
        SIGNAL Clk :  std_logic := '0';
        SIGNAL Rst :  std_logic := '0';
        SIGNAL T :  std_logic := '0';
        SIGNAL Q :  std_logic;

BEGIN
        -- Instantiate the Unit Under Test (UUT)
        uut: TFF_Syn PORT MAP(
                Clk => Clk,
                Rst => Rst,
                T => T,
                Q => Q
        );
        Clk<= not Clk after 10ns;
        Rst<='1' after 40ns;
```

```
        T<='1' after 10ns,'0' after 30ns;
END;                                                    64
```

Result: **T Flip Flop with Synchronous "Reset"** is designed using VHDL and simulated the same using Xilinx ISE Simulator

Schematic Diagram:



Synthesis Report

HDL Synthesis Report

Macro Statistics

Counters : 1
4-bit up counter : 1

Final Register Report

Macro Statistics
Registers : 4
Flip-Flops : 4

Final Report:

Final Results
RTL Top Level Output File Name : BCD_Counter_Asyn.ngr
Top Level Output File Name : BCD_Counter_Asyn
Output Format : NGC
Optimization Goal : Speed
Keep Hierarchy : NO

Design Statistics

IOs : 6

Cell Usage :

BELS : 4
INV : 1
LUT2 : 1
LUT3 : 1

```
#      LUT4                : 1
# FlipFlops/Latches        : 4
#      FDC                 : 4
# Clock Buffers            : 1
#      BUFGP               : 1
# IO Buffers               : 5                    65
#      IBUF                : 1
#      OBUF                : 4
=========================================================================
```

Experiment No:14 Counter with Asynchronous Reset

Aim: To Design **BCD Counter with Asynchronous Reset** using VHDL and simulate the same using Xilinx ISE Simulator

Tools Required: 1.PC

2. Xilinx ISE

VHDL Code:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
entity BCD_Counter_Asyn is
   Port ( Rst : in  STD_LOGIC;
          Clk : in  STD_LOGIC;
          Count : Buffer  STD_LOGIC_VECTOR (3 downto 0));
end BCD_Counter_Asyn;
architecture Behavioral of BCD_Counter_Asyn is
begin
   process(Rst,Clk,Count)
   begin
      if Rst='1' then Count<="0000";
     elsif Clk'event and clk='1' then
     Count<=Count+1;
     if count="1111" then count<="0000";
    end if;
```

```
    end if;
  end process;
end Behavioral;
```

Device utilization summary:

Selected Device : 3s250eft256-5

Number of Slices:	2	out of 2448	0%
Number of Slice Flip Flops:	4	out of 4896	0%
Number of 4 input LUTs:	4	out of 4896	0%
Number of IOs:	6		
Number of bonded IOBs:	6	out of 172	3%
Number of GCLKs:	1	out of 24	4%

TIMING REPORT:

Clock Information:

Clock Signal	Clock buffer(FF name)	Load
Clk	BUFGP	4

Asynchronous Control Signals Information:

Control Signal	Buffer(FF name)	Load
Rst	IBUF	4

Timing Summary:

Speed Grade: -5

Minimum period: 2.289ns (Maximum Frequency: 436.862MHz)

Minimum input arrival time before clock: No path found

Maximum output required time after clock: 4.221ns

Timing constraint: Default period analysis for Clock 'Clk'
Clock period: 2.289ns (frequency: 436.862MHz)
Total number of paths / destination ports: 10 / 4

Delay: 2.289ns (Levels of Logic = 1)
Source: Count_0 (FF)
Destination: Count_0 (FF)
Source Clock: Clk rising
Destination Clock: Clk rising

Data Path: Count_0 to Count_0

Cell:in->out	fanout	Gate Delay	Net Delay	Logical Name (Net Name)
FDC:C->Q	5	0.514	0.538	Count_0 (Count_0)
INV:I->O	1	0.612	0.357	Mcount_Count_xor<0>11_INV_0 (Mcount_Count)
FDC:D		0.268		Count_0
Total		2.289ns		

Timing constraint: Default OFFSET OUT AFTER for Clock 'Clk'

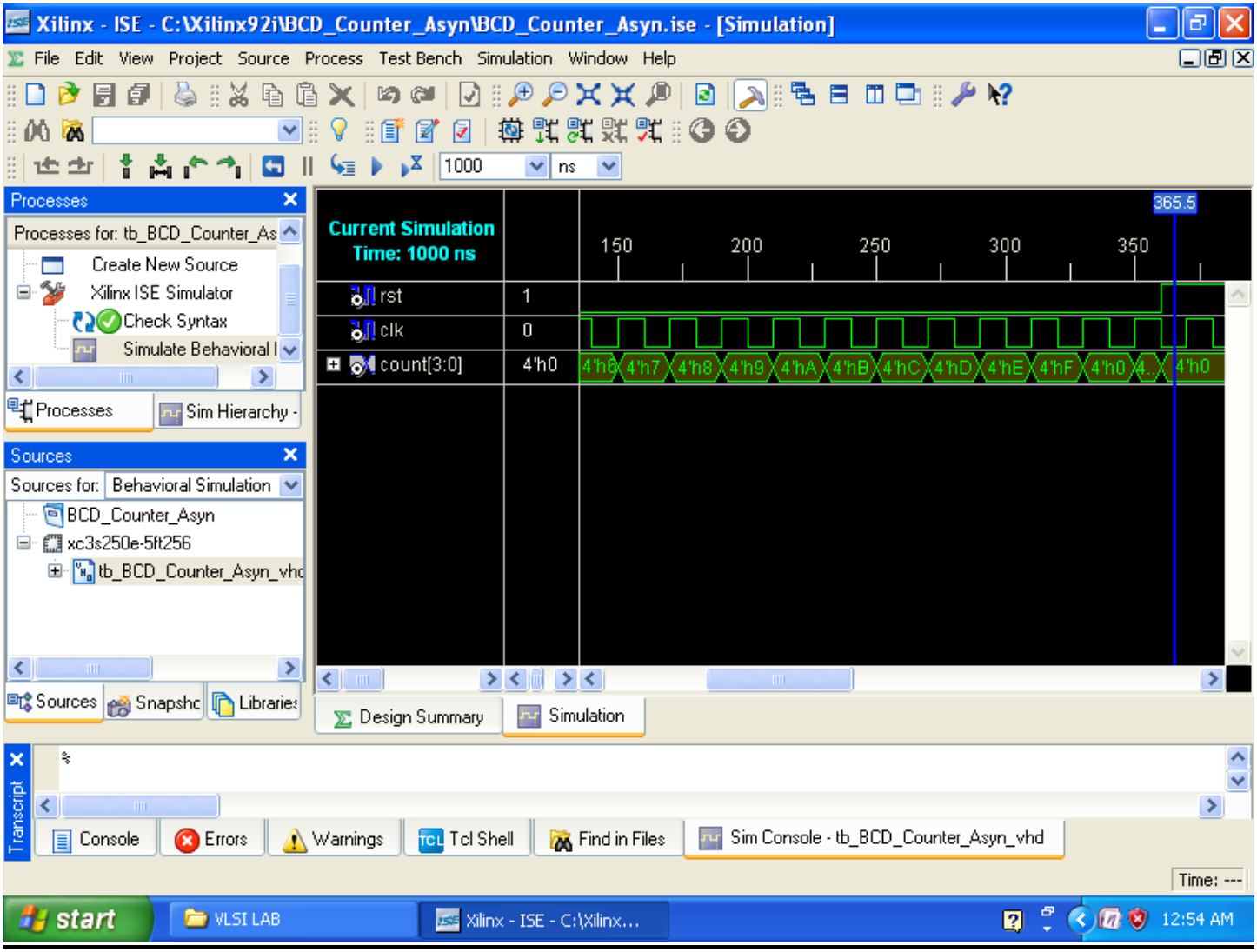
Total number of paths / destination ports: 4 / 4

Offset: 4.221ns (Levels of Logic = 1)
Source: Count_0 (FF)
Destination: Count<0> (PAD)
Source Clock: Clk rising

Data Path: Count_0 to Count<0>

Cell:in->out	fanout	Gate Delay	Net Delay	Logical Name (Net Name)
FDC:C->Q	5	0.514	0.538	Count_0 (Count_0)
OBUF:I->O		3.169		Count_0_OBUF (Count<0>)
Total		4.221ns		

Simulation Results:

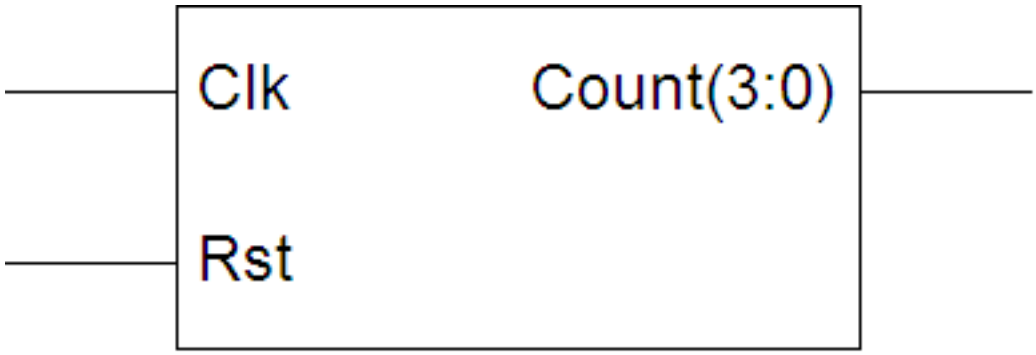

Xilinx - ISE - C:\Xilinx92i\BCD_Counter_Asyn\BCD_Counter_Asyn.ise - [Simulation]
File Edit View Project Source Process Test Bench Simulation Window Help
1000 ns
Processes
Processes for: tb_BCD_Counter_As
Create New Source
Xilinx ISE Simulator
Check Syntax
Simulate Behavioral I
Processes
Sim Hierarchy -
Sources
Sources for: Behavioral Simulation
BCD_Counter_Asyn
xc3s250e-5ft256
tb_BCD_Counter_Asyn_vhc
Sources
Snapshc
Libraries
Current Simulation Time: 1000 ns
365.5
150
200
250
300
350
rst
1
clk
0
count[3:0]
4'h0
4'h6
4'h7
4'h8
4'h9
4'hA
4'hB
4'hC
4'hD
4'hE
4'hF
4'h0
4'h0
Design Summary
Simulation
Transcript
Console
Errors
Warnings
Tcl Shell
Find in Files
Sim Console - tb_BCD_Counter_Asyn_vhd
Time: ---
start
VLSI LAB
Xilinx - ISE - C:\Xilinx...
12:54 AM

VHDL Test bench:

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.std_logic_unsigned.all;
USE ieee.numeric_std.ALL;
ENTITY tb_BCD_Counter_Asyn_vhd IS
END tb_BCD_Counter_Asyn_vhd;
ARCHITECTURE behavior OF tb_BCD_Counter_Asyn_vhd IS
        -- Component Declaration for the Unit Under Test (UUT)
        COMPONENT BCD_Counter_Asyn
        PORT(
                Rst : IN std_logic;
                Clk : IN std_logic;
                Count :Buffer std_logic_vector(3 downto 0)
                );
        END COMPONENT;
        --Inputs
        SIGNAL Rst :  std_logic := '0';
        SIGNAL Clk :  std_logic := '0';
        --Outputs
        SIGNAL Count :  std_logic_vector(3 downto 0);
BEGIN
        -- Instantiate the Unit Under Test (UUT)
        uut: BCD_Counter_Asyn PORT MAP(
                Rst => Rst,
                Clk => Clk,
                Count => Count
        );
        Clk<= not clk after 10ns;
        Rst<='1' after 10ns,'0' after 20ns,'1' after 360ns;
END;
```

Result: BCD Counter with Asynchronous Reset is designed using VHDL and simulated the same using Xilinx ISE Simulator

Schematic Diagram:



Experiment No:15 BCD Counter with Asynchronous Reset

Aim: To Design **BCD Counter with Synchronous Reset** using VHDL and simulate the same using Xilinx ISE Simulator

Tools Required: 1.PC

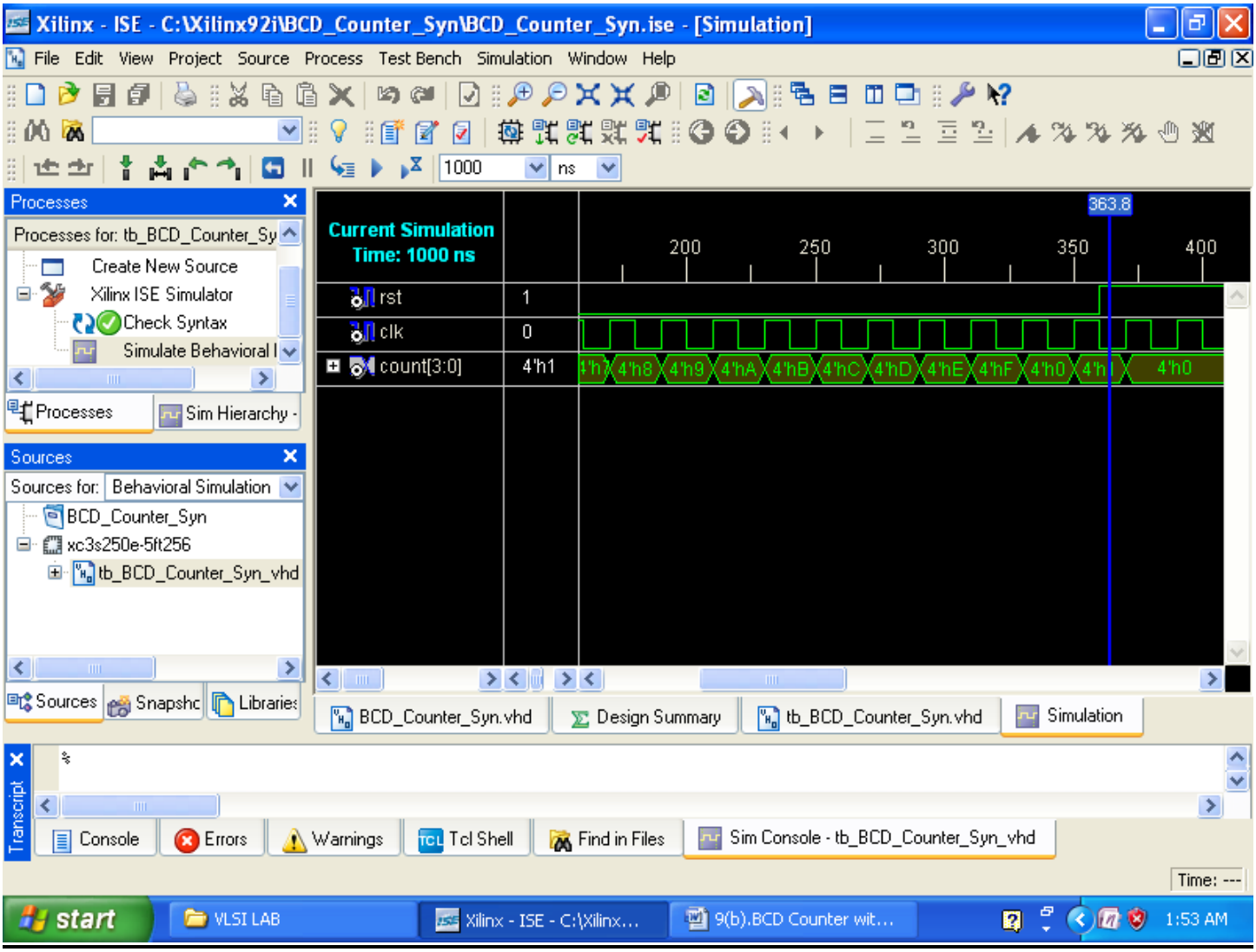
2. Xilinx ISE

VHDL Code:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
entity BCD_Counter_Syn is
   Port ( Rst : in  STD_LOGIC;
          Clk : in  STD_LOGIC;
          Count : Buffer  STD_LOGIC_VECTOR (3 downto 0));
end BCD_Counter_Syn;
architecture Behavioral of BCD_Counter_Syn is
begin
   process
   begin
      wait until clk'event and clk='1';;
      if Rst='1' then Count<="0000";
     elsif Clk'event and clk='1' then
     Count<=Count+1;
     if count="1111" then count<="0000";
    end if;
    end if;
```

```
        end process;
    end Behavioral;
```

Simulation Results:



VHDL Test bench:

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.std_logic_unsigned.all;
USE ieee.numeric_std.ALL;
ENTITY tb_BCD_Counter_Syn_vhd IS
END tb_BCD_Counter_Syn_vhd;
ARCHITECTURE behavior OF tb_BCD_Counter_Syn_vhd IS
        -- Component Declaration for the Unit Under Test (UUT)
        COMPONENT BCD_Counter_Asyn
        PORT(
                Rst : IN std_logic;
                Clk : IN std_logic;
                Count :Buffer std_logic_vector(3 downto 0)
                );
        END COMPONENT;
        --Inputs
        SIGNAL Rst :  std_logic := '0';
        SIGNAL Clk :  std_logic := '0';
        --Outputs
        SIGNAL Count :  std_logic_vector(3 downto 0);
```

```
BEGIN
        -- Instantiate the Unit Under Test (UUT)
        uut: BCD_Counter_Asyn PORT MAP(
                Rst => Rst,
                Clk => Clk,
                Count => Count
        );
        Clk<= not clk after 10ns;
        Rst<='1' after 10ns,'0' after 20ns,'1' after 360ns;
END;
```

Result: BCD Counter with Synchronous Reset is designed using VHDL and simulated the same using Xilinx ISE Simulator