Department of

Electrical Engineering

LAB MANUAL

ELECTRONIC CIRCUITS LAB

B.Tech– IV Semester

KCT College OF ENGG AND TECH.
VILLAGE FATEHGARH
DISTT.SANGRUR

INDEX

EXPERIMENT-1 NAND AND NOR GATES

Aim: Realization of logic gates using NAND and NOR gates.

Apparatus :-

1. Fixed output regulated power supply of 5V.
2. Two logic '0'& two logic '1' inputs with output provided on Sockets.
3. Red output indicators is provided on the front panel to observe the output status.
4. Four NAND & Four NOR gates are printed on the front panel, IC's placed inside the cabinet & connections for input & output are brought out on socket.

Theory:

To build logic circuit, OR gate is used for addition sign, AND gate is used for multiplication sign & NOT gate is used for inverse sign. Hence AND' OR' NOT logic gates are basic building blocks logic circuits. NAND gates & NOR gates can be used to build AND, OR, NOT gates. Hence NAND gates & NOR gates are called universal building block of logic gates.

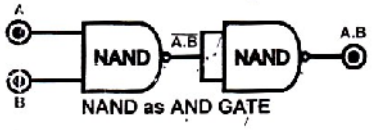
Procedure: **Verification of 'NAND' as 'AND' gate**

1. Connect 'A' & 'B' inputs of "AND" gate to logic inputs '0'& '1' as shown in the truth table for "AND" gate to logic indicator.
2. Switch ON the instrument using ON/OFF Toggle switch provided on the front panel.
3. Check the output indicator. If it glows the indication is that the output is in the state "1" & if it does not glow the indication is that output is in state '0".
4. Similarly verify the input for other combination of input "A" & "B" as shown in the truth cable.

NAND as NOT GATE

"NOT" GATE

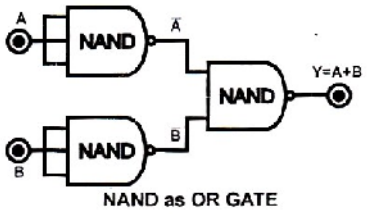
A	Y
0	1
1	0



NAND as AND GATE

"AND" GATE

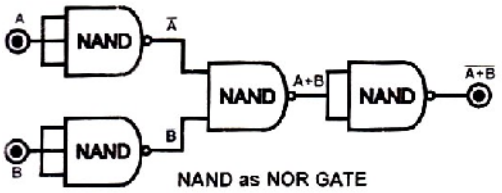
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1



NAND as OR GATE

"OR" GATE

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1



NAND as NOR GATE

"NOR" GATE

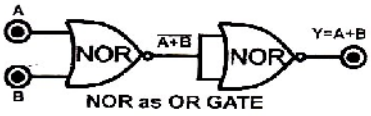
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Verification of 'NOR' as other gates

NOR as NOT GATE

"NOT" GATE

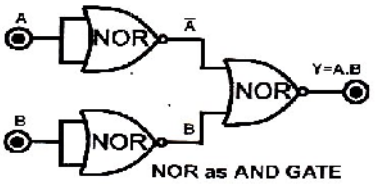
A	Y
0	1
1	0



NOR as OR GATE

"OR" GATE

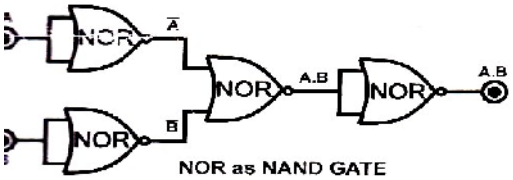
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1



NOR as AND GATE

"AND" GATE

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1



NOR as NAND GATE

"NAND" GATE

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

RESULT:NAND gate and NOR gate as other gates are verified.

EXPERIMENT-2 TRUTH TABLE FOR D FLIP FLOP

Aim: Verification of truth table for D flip flop.

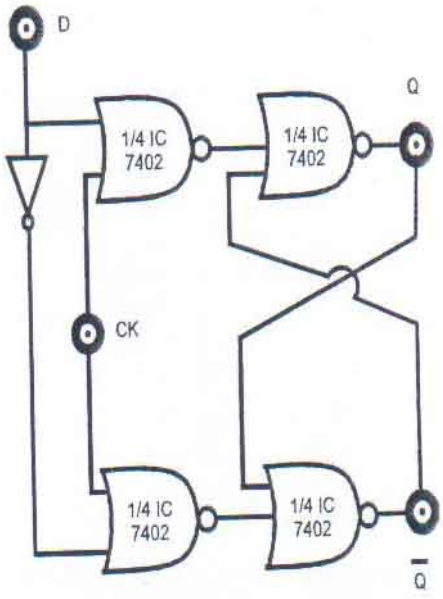
Apparatus Required:

1. Fixed output regulated power supply of 5V.
2. 1Hz Mono shot clock pulse with pulsar switch is provided on the front panel.
3. One logic inputs logic '0'& logic '1' selectable using SPDT switches are provided on the front panel.
4. Two red output indicators are also provided on the front panel
5. IC 7402 is mounted on the front panel,7 important connections are brought out on sockets.

Theory:

A flip flop is an electronic circuit that has two stable states , one representing a binary '1' & the other binary '0' .if one put into one state , the flip flop will remain in that state as long

as power is applied or until it is changed . In digital circuits flip flops are used in variety of storage, counting, sequencing & timing applications. The 'D' flip flop has two outputs that determine whether it is storing a binary '1' & the other binary '0'. It also has two inputs. These are called 'D' and 'T' and work differently. The data or bit to be stored is applied to the 'D' input. The 'T' input line controls the flip flop . it is used to determine whether the input data at 'D' is to be recognized or ignored . if the 'T' input is high , the data on the 'D' line get stored in the flip flop. If the 'T' line is low the 'D' input line data has no effect and bit stored previously is retained.



Procedure:

1. Connect the output of logic inputs to 'D' input of the flip flop. Also connect 'Q' outputs to the output indicator.
2. Connect 1Hz clock output to the 'clock' input of the flip flop.
3. Switch ON the instrument using ON/OFF toggle switch provided on the front panel.
4. Verify the truth table of input combinations.

Observation Table:

INPUTS		OUTPUTS	
CLOCK(CK)	D	Q	Q'

1 1	1 0	1 0	0 1

Result:

The truth tables for NOR gate latch is verified.

EXPERIMENT-3 IC FLIP FLOPS (D LATCH, D FLIP FLOP, JK FLIP FLOPS)

Aim: Verification of truth table for IC flip flops (D Latch, D flip flop, JK flip flops).

Apparatus:

1. D type flip flop using TTL IC 7474.
2. JK flip flop using TTL IC 7676.
3. D latch using IC 7400.
4. Fixed output DC regulated Power Supply of 5V.
5. 1Hz monoshot clock pulse with pulser switch.
6. Four logic inputs logic '0' & logic '1' selectable using SPDT switches.
7. Two red output indicators.
8. IC 7400, 7474 & 7476.
9. Single and double patch cards.

Theory:

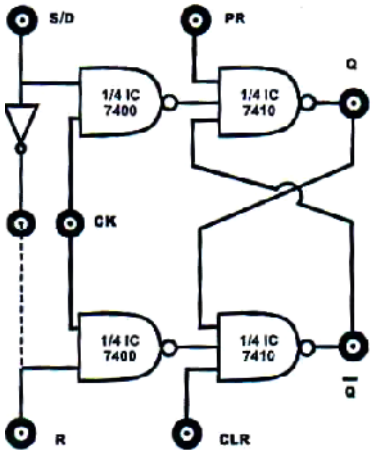
A flip flop is electronic circuit that has two stable states, one representing a binary '1' and the other binary '0'. In digital circuits, flip flops are used in a variety of storage, counting, sequencing and timing applications. There are three basic types of flip flops, the set-reset (also known as 'R-S flip flop or a latch), the 'D' type and the 'JK'. The 'RS' flip flop is the simplest.

The 'D' flip flop has two outputs that determine whether it is storing a binary '1' or a binary '0'. It also has two inputs. There are called 'D' and 'T' and work differently.

The 'JK' flip flop is the most versatile binary storage element. It can perform all the functions of 'R', 'S' and 'D' flip flops plus it can do several other things. An integrated circuit 'JK' flip flop is really two 'RS' flip flops in one. These are called Master and Slave. Both flip flops are controlled by a common clock pulse to the 'T' input.

Procedure: Verification of 'D' Latch:

1. Connect the output of NOT Gate to 'R' input through patchcord. Connect 3 logic inputs to 'Preset (PR)', Clear (CR)' & 'D' input of the flip-flop as shown in fig. through patchcords. Also connect 'Q' & 'Q' outputs to output indicators.



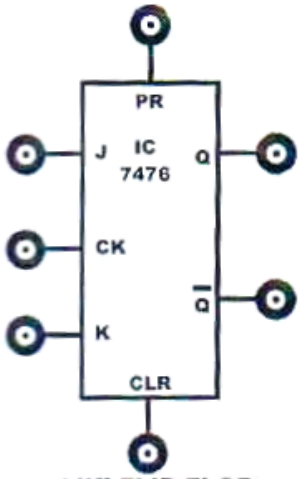
'D' TYPE FLIP FLOP

TRUTH TABLE 'D' FLIP FLOP

INPUTS				OUTPUTS	
PRESET (PR)	CLEAR (CR)	CLOCK (CK)	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	P	H	H	L
H	H	P	L	L	H

2. Connect 1Hz clock output to 'Clock (CK)' input of the flip flop.

Verification of 'JK' Flip Flop:



'JK' FLIP FLOP

TRUTH TABLE 'JK' FLIP FLOP

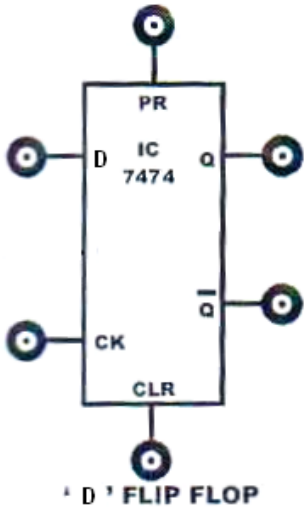
INPUTS					OUTPUTS	
PRESET (PR)	CLEAR (CR)	CLOCK (CK)	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H	H
H	H	P	L	L	Q_0	$\overline{Q_0}$
H	H	P	H	L	H	L
H	H	P	L	H	L	H
H	H	P	H	H	TOGGLE	

1. Connect the 4 Logic inputs to 'Preset (PR)', Clear (CR)', 'J' & 'K' input of the Flip-Flop as shown in fig. through patchcords. Also connect 'Q' & 'Q'' outputs to output indicators.
2. Connect 1Hz clock output to 'Clock (CK)' input of the flip flop.
3. Switch ON the instrument using ON/ OFF toggle switch provided on the front panel.
4. Verify the Truth Table for various sets of input combinations.

Verification of 'D' Type Flip Flop:

1. Connect the 3 Logic inputs to 'Preset (PR)', Clear (CR)' & 'D' input of the Flip-Flop as shown in fig. through patchcords. Also connect 'Q' & 'Q' outputs to output indicators.
2. Connect 1Hz clock output to 'Clock (CK)' input of the flip flop.
3. Switch ON the instrument using ON/ OFF toggle switch provided on the front panel.

4. Verify the Truth Table for various sets of input combinations.



'D' FLIP FLOP

TRUTH TABLE 'D' FLIP FLOP

INPUTS				OUTPUTS	
PRESET (PR)	CLEAR (CR)	CLOCK (CK)	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	P	H	H	L
H	H	P	L	L	H

Result:

The truth tables for D Latch, D flip flop, JK flip flops are verified.

EXPERIMENT-4 **ASYNCHRONOUS 4 BIT DECADE COUNTER USING IC 7490**

Aim: Verification of truth table for Asynchronous 4 bit decade counter using IC 7490.

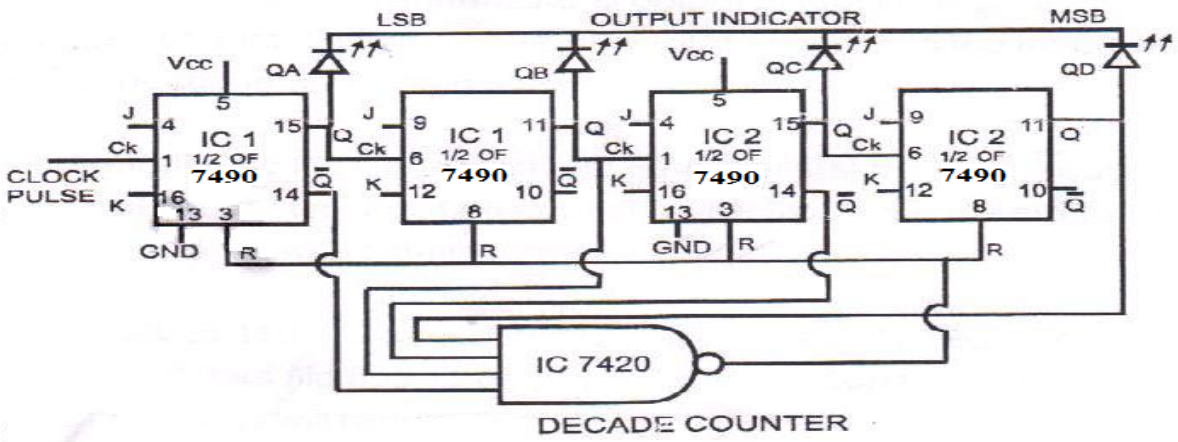
Apparatus:

1. Fixed output DC regulated power supply 5V DC.
2. Monoshot clock pulse of 1Hz, seven single point patch cords for connection.
3. Four output logic indicator.
4. IC 7476 is placed inside & connections are brought out on sockets.

Theory:

4 bit ripple counter counts upto 15 & then resets to '0'. But it can be made to reset to at any clock pulse. For this purpose we operate the reset connections automatically using 4 input NAND gate. as you know that output of a NAND gate is low if & only if all the inputs are high .Suppose we want to convert 4-bit forward counter to decade counter .For Decade counter it is required that counter should count up to 9 & than resets to zero at tenth clock pulse . We know that at a tenth clock pulse output of 2^{nd} & 4^{th} flip flop is high & output of 1^{st} & 3^{rd} flip flop is low. So we choose Q output of 2^{nd} & 4^{th} flip flop & Q` output of 1^{st} & 3^{rd} flip flop for the nputs for the inputs of 4-input NAND gate. Also Connect output of NAND gate to common reset pin of all the flip flops. As you can program the counter for any number of pulses that is why this counter is known as Modulo Counter.

Circuit Diagram:



CLOCK	Q_D	Q_C	Q_B	Q_A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

Procedure:

1. Connect the circuit as shown. Through patch cords i.e. connect clock output to ck (clock pulse) input of first flip flop , connect Q output of first flip flop to ck input of second flip flop , Q output of second flip flop to ck input of third flip flop , Q output of third flip flop

to ck input of fourth flip flop as shown. Also connect all the all four Q outputs to output indicators Connect the Q` output of first flip flop , Q` output of second flip flop , Q output of third flip flop, Q output of fourth flip flop to the inputs of NAND gate.

2. Keep all the J & K inputs open, as in open condition they assume to be in state '1'.
3. Switch ON the instrument using ON/OFF toggle switch provided on the front panel.
4. For counting, apply clock pulses one by one using pulser switch. Note down all the four outputs at the application of each pulse & verify the truth table.

Result:

The truth table of Asynchronous 4 bit decade counter is verified.

EXPERIMENT-5 CLIPPERS & CLAMPERS

Aim :- To study different waveforms of clippers & clampers.

Appartus :-Function Generator(1 MHz), CRO(30 MHz), probes, Connecting Wires, Diode IN4007, Resistor 1KΩ, Capacitor 0.1μf.

Clippers

It is frequently necessary to modify the shape of various waveforms for use in instrumentation, controls, computation, and communications. Wave shaping is often achieved by relatively simple combination of diodes, resistors, and voltage sources. Such circuits are called clippers, limiters, amplitude selectors, or slicers. Clipper circuits are primarily used to prevent a waveform from exceeding a particular limit, either positive or negative. For example, one may need to limit a power supply's output voltage so it does not exceed +5 V. The most widely used wave shaping circuit is the rectifier, which you have previously studied. Fig. shows a positive clipper circuit.

Circuit Diagram :-

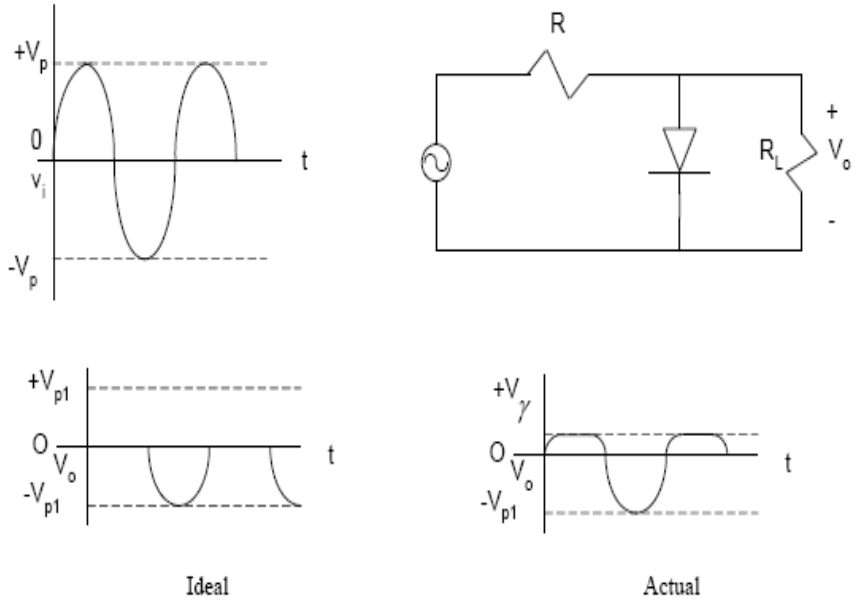


Fig. A positive clipper circuit: (a) Sinusoidal input to clipper circuit; (b) A positive clipper circuit; (c) Output of ideal positive clipper and (d) Output of actual positive clipper circuit

As indicated, the output voltage has the entire positive half-cycles clipped off. The circuit works as follows: During the positive half-cycle of the input voltage, the diode turns on. For an ideal

diode, the output voltage is zero. For an actual diode the output voltage is equal to Vγ , the cut-in voltage of the diode. During the negative half-cycle, the diode is reverse-biased and can be approximated by an open circuit. In many clippers, the load resistor, RL, is much larger than the series resistor, R. In which case, essentially all of the negative half-cycle voltage appears at the output through voltage-divider action. If RL and R are comparable, then on the negative half-cycle, the output voltage would be given by

$$Vo = Vp1 = Vp \bullet (RL / (RL + R)).$$

Since the first Vγ volts are used to begin conduction in the diode, the output signal is clipped near Vγ, rather than at 0V. If the diode polarity is reversed, the result is a negative clipper that removes the negative half cycle. In this case, the clipping levels occur near -Vγ.

Clampers

In certain instances, it may be desirable to keep the output waveform essentially unchanged, but modify its dc level to some required value. This can be done by the use of diodes, resistors, capacitors, and voltage sources. Such circuits are known as clampers. For example, if the input voltage signal swings from -10V to +10V, a positive dc clamper can produce an output that keeps the signal wave shape intact but swings the voltage from 0V to +20V. TV receivers use a dc clamper to add a dc voltage to the video signal. Here the dc clamper is usually called a dc restorer. In Figure a positive dc clamper is shown. The clamper operates as follows: During the negative half-cycle of the input voltage, the diode turns on as illustrated in Figure. At the negative peak, the capacitor charges up to Vp with the polarity shown and the output voltage iszero. As the voltage grows beyond the negative peak, the diode shuts off as shown in Fig.

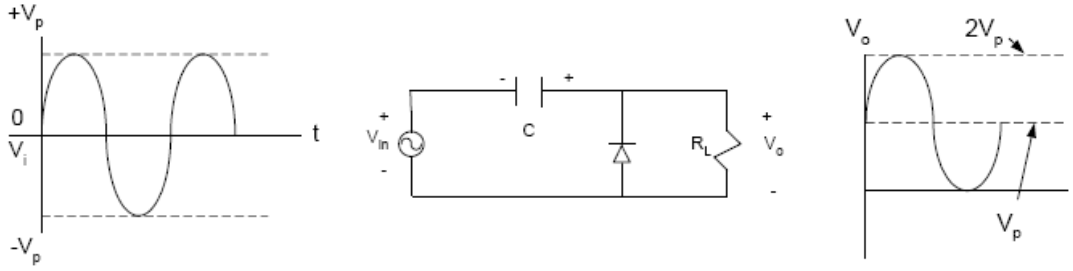


Fig:- Positive dc clamper: (a) Sinusoidal input to positive dc clamper; (b) Positive dc clamper; and (c) Clamped sinusoidal output

The capacitor retains the voltage for a short time. The RLC time constant is deliberately made much larger than the period, T, of the input signal. Hence, the capacitor remains almost fully charged during the entire off time of the diode. The capacitor thus acts like a battery of Vp volts and now only passes the ac signal, which rides on top of VP. The output voltage signal, therefore, consists of the input signal riding on a dc voltage of +Vp volts. Since the diode drops Vγ volts when conducting, the capacitor voltage does not quite reach +Vp volts. For this reason, the dc clamping is not perfect, and the negative peaks are at -Vγ as shown in Fig. When the polarity of the diode in Fig. is reversed, the polarity of the capacitor voltage reverses also, and the circuit becomes a negative dc clamper. Ideally, the output voltage consists of the input voltage riding on a dc voltage of -Vp volts. If the diode is considered nonideal, then the output will consist of the input signal riding on a dc voltage of -(Vp-Vγ) volts, and the positive peaks will occur at Vγ volts.

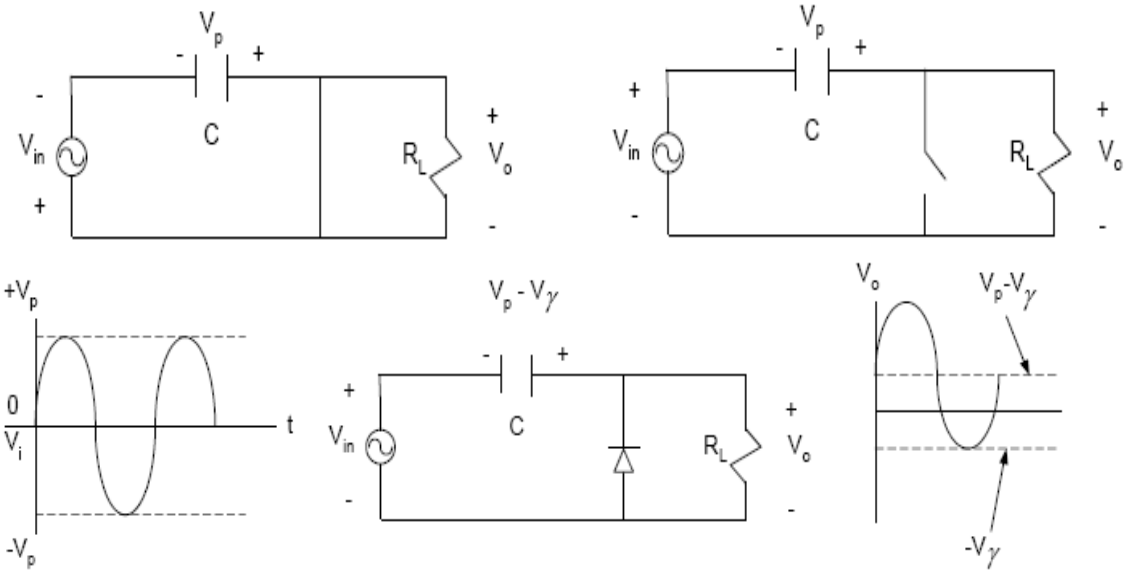


Fig: Positive clamping circuit operation

From the above discussions, it can be seen that when the diode points upward, a positive dc clamper results. When the diode points downward, the circuit is a negative dc clamper. The clamping value can be modified by putting a voltage source V_B in series with the diode, shifting the peak voltage to ($\pm V_\gamma \pm V_B$), depending on the sign of V_B and the polarity of the diode.

Results

1. **Ideal Clipping Circuits** — Build 4 circuits

a. **V_{in} = 8V_{P-P}, 1kHz, V_B = 0 & 2V**.

b. Sketch the input and output waveforms.

c. Record the voltage at which clipping occurs.

2. **Series-Biased Clippers** — Build 4 circuits

a. **V_{sin} = 8V_{P-P}, 1 kHz, V_B = 0 & 2V**.

b. Sketch the input and output waveforms.

c. Record the voltage at which clipping occurs.

3. **Parallel-Biased Clipper** — Build circuit

a. **V_{in} = 8V_{P-P}, 1kHz, V_{B1} and V_{B2} = 2V**.

b. Sketch the input and output waveforms.

c. Record the voltage at which clipping occurs.

4. Clamper — Build circuit

a. **V_{in} = 8V_{P-P}, 1kHz, V_{dc} = 2V**.

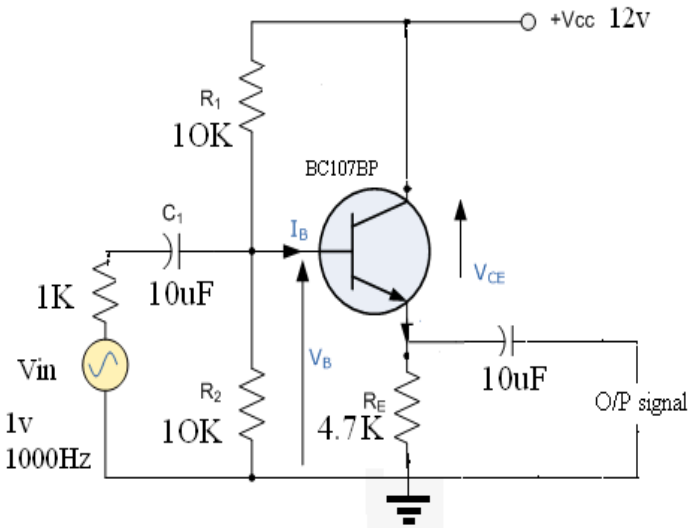
b. Sketch the input and output waveforms.

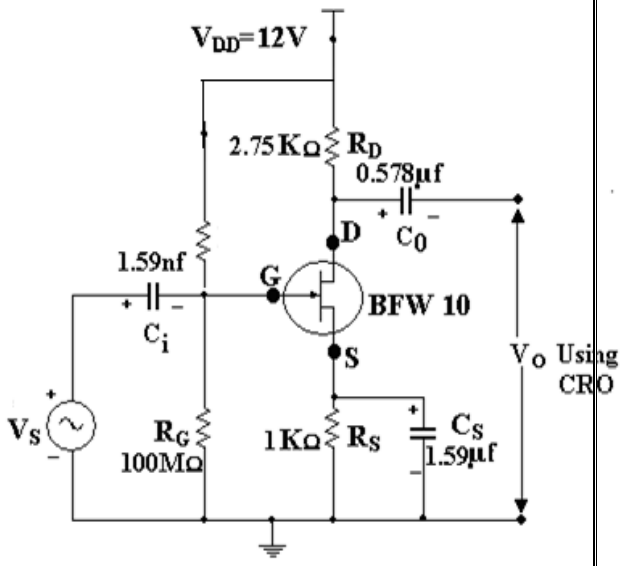
EXPERIMENT-6

Aim: Measurement of Parameters of Emitter Follower and Source Follower; R_I, A_V, A_I &R_o.

Apparatus: FETBFW10, Transistor BC107, Resistors, Capacitors, CRO, Function Generator, Multi meter.

CIRCUIT DIAGRAM:





THEORY:

EMITTER FOLLOWER

The common collector circuit is also known as emitter follower. The ac output voltage from a CC circuit is essentially the same as the input voltage; there is no voltage gain or phase shift. Thus, the CC circuit can be said to have a voltage gain of 1. The fact that the CC output voltage follows the changes in signal voltage gives the circuit its other name emitter follower. The input impedance of a CC amplifier is high. Output impedance is low and the
Voltage gain is almost unity. Because of these Characteristics the CC circuit is normally used as a buffer amplifier, placed between a high impedance signal source and a low impedance load.

SOURCE FOLLOWER

The FET common drain circuit has the output voltage developed across the source resistor Rs. Here the ac output voltage is closely equal to the ac input voltage, and the circuit can be said to have unity gain. Because the output voltage at the source terminal follows the signal voltage at the gate, the common drain circuit is also known as a source follower. A common drain circuit has a voltage gain approximately equal to 1, no phase shift between input and output, very high input impedance and low output impedance. Because of its high Zi, low Zo and unity gain the CD circuit is used as a buffer amplifier between a high impedance signal source and a low impedance load.

PROCEDURE:

1. Connect the circuit as per the circuit diagram.
2. Apply Vslv 1 KHz signal from the signal generator.
3. Observe corresponding output from the CRO and then calculate voltage gain using the formula Av=Vo/Vi.
4. Measure voltage across AB terminals and then calculate input current by using the formula $Iin=V_{ab}/R_{ab}$.
5. Measure current flowing through resistor at Source (or Emitter) terminal and note down it as Iout.
6. Calculate Current gain using the formula $AI=Iin/I_{out}$.
7. Calculate input resistance using the formula Rin=Vin/Iin.
8. To calculate the output resistance, connect the pot at the output and vary the resistance of the pot up to half of
the output with RL is equal to infinity. The resistance of pot is the output resistance.

PRECAUTIONS:

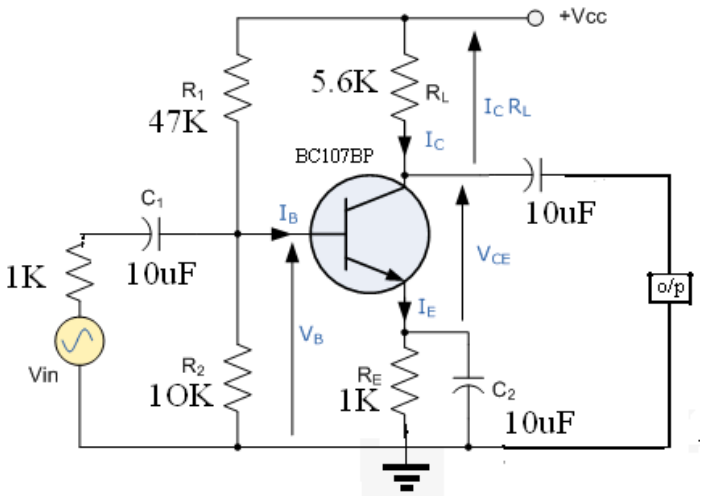
1. Wires should be checked for good continuity
2. FET terminals must be identified and connected carefully.

EXPERIMENT-7

Aim :- To obtain the frequency response of an amplifier and calculate the gain bandwidth of the amplifier.

Apparatus:- Transistor BC107, Resistors, Capacitors, CRO, Signal generator.

Circuit Diagram :-



Theory:-

The CE amplifier is a small signal amplifier. This small signal amplifier accepts low voltage ac inputs and produces amplified outputs. A single stage BJT circuit may be employed as a small signal amplifier; has two cascaded stages give much more amplification. Designing for a particular voltage gain requires the use of a ac negative feedback to
stabilize the gain. For good bias stability, the emitter resistor voltage drop should be much larger than the base -emitter voltage. And R_e resistor will provide the required negative feedback to the circuit. C_E is provided to provide necessary gain to the circuit. Allbypass capacitors should be selected to have the smallest possible capacitance value, both to minimize the physical size of the circuit for economy. The coupling capacitors should have a negligible effect on the frequency response of the circuit.

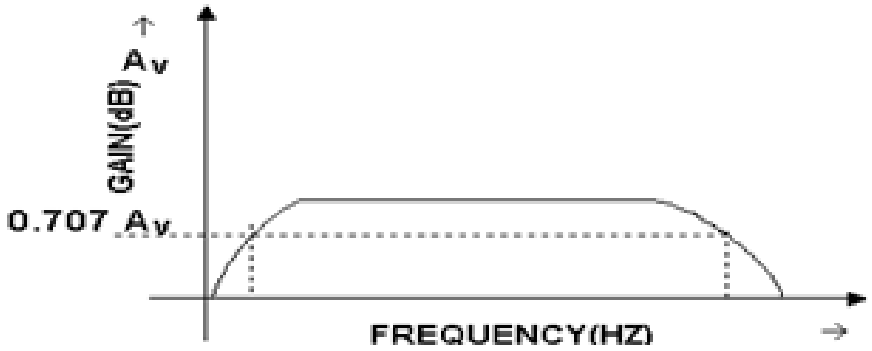
Procedure:-

1. Connect the circuit as per the circuit diagram.
2. Give l00Hz signal and 20mv p-p as Vs from the signal generator
3. Observe the output on CRO and note down the output voltage.
4. Keeping input voltage constant and by varying the frequency in steps 100Hz-1MHz, note down the corresponding output voltages.
5. Calculate gain in dB and plot the frequency response on semi log sheet

TABULAR FORM:- Input voltage (Vi)=

NO.	FREQUENCY	OUTPUT VOLTAGE(Vo)	GAIN Av=Vo/Vi	GAIN IN dB 20 log gain

Model Graph:-



Precautions:

1. Wires should be checked for good continuity.
2. Transistor terminals must be identified and connected carefully.

EXPERIMENT-8

Aim :- To study the Class B and Class AB amplifier.

Apparatus:-

1. Digital multimeter (Fluke 8010A, BK PRECISION 2831B).
2. Function Generator Wavetek FG3B.
3. Digital oscilloscope Tektronix TDS 210.
4. MJE800 NPN and MJE700 PNP Darlington transistors.
5. 1N4148 diodes – 3.
6. C=47 uF – 2; C=470uF – 1.
7. R=8.2 uF / 2W.

Procedure:-

1. You are provided with two heat sinks, which should be attached to the transistors during the lab exercise. The heat sink supposed to be electrically insulated from the collector of the transistor, however it is always recommended to avoid any contact of the heat sinks to the ground or to each other. Occasionally check the temperature of the heat sink, if you cannot keep your finger of the heat sink for more than twenty seconds the transistors may be too hot. Shut the power off and check your circuit.

2. Connect the **class B** power amplifier shown in Fig. using MJE800 NPN and MJE700 PNP Darlington transistors instead of single BJTs. Use the R_L= 8.2 Ω resistor to replace the loudspeaker's load.

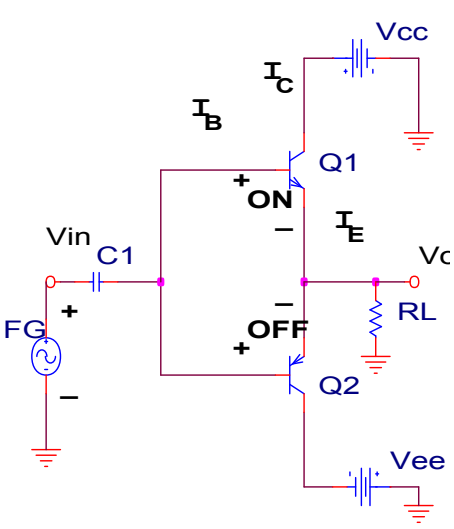
3. Use a dual voltage Power Supply and connect its POS terminal as Vcc, NEG terminal as Vee and COM terminal as a common ground. Set the power supply voltage to 6V DC. Measure the DC quiescent point values. Compare the voltages and currents from simulation with the experimental data in a Table 2.1. If your results are significantly different (more than 15%) from your simulated values, try to find out and eliminate the reason for that discrepancy.

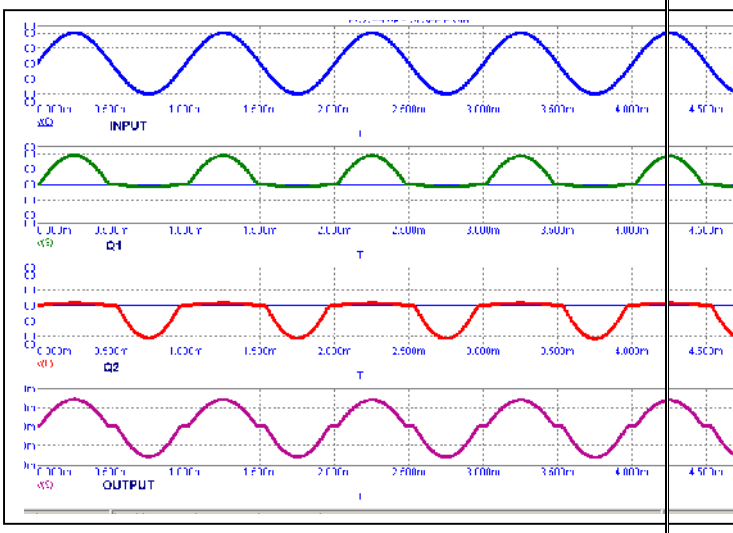
4. Once you are satisfied that your circuit is biased correctly, then connect the signal generator to the input. Set the signal generator to a frequency of 1 kHz. For the input signal level of Vin = $3V_{rms}$ (~4Vp) sketch the output voltage across the 8.2 Ω load on top of your MicroCap simulation plot. Compare the simulated and experimental waveforms and explain the differences if any.

5. Increase the input sinusoidal voltage until you notice a clipping in the output voltage. Record this value and compare with DC power supply voltages. For these readings you can use the BK Precision meter to measure the AC input current (it measures the RMS value), measure the input voltage after the digital meter (scope) as it is shown in Figure 2.6.

6. For the input signal Vin= 2 V_{rms} and Vin=1.8V_{rms} calculate the input AC power P_{in}, the output AC power P_o, the DC input power from the DC supply P_{DC}. Also calculate the AC voltage gain A_V [dB], the AC power gain [dB] and the amplifier efficiency of the class B power amplifier.

Circuit Diagram:-





a) Positive half cycle operation b) Class B output waveforms

Fig. Class B power amplifier operation

Power Amplifier Class B

Class B amplification involves using a dual voltage power supply along with two power transistors, an NPN, and its complementary PNP device. Such a circuit is shown in Fig. and its operation could be explained as following:

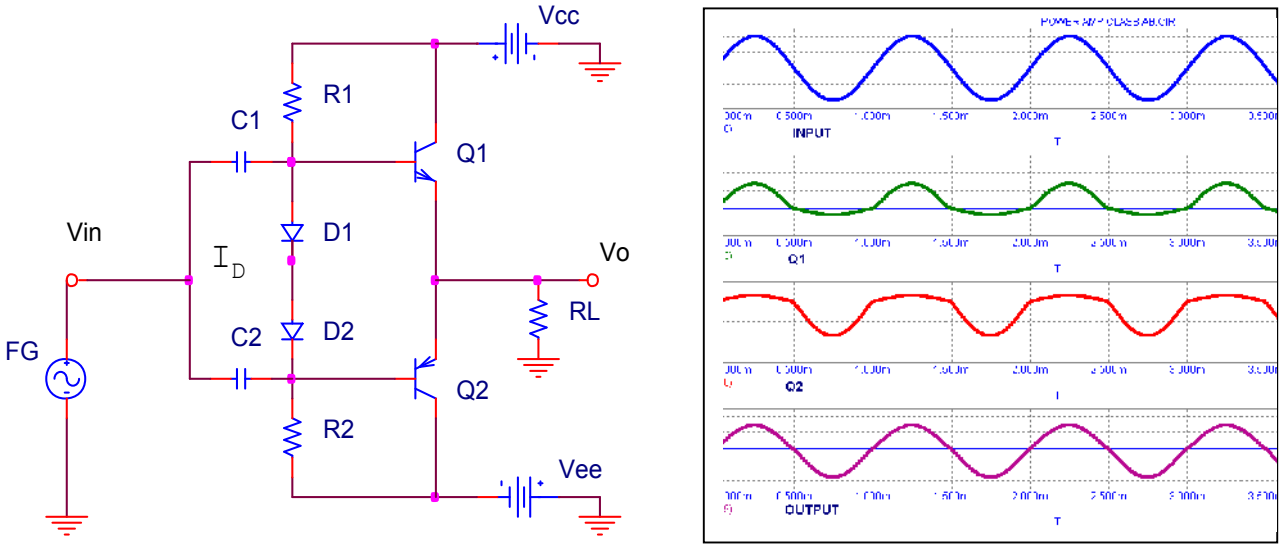
- In the absence of an input signal, neither transistor conducts; both transistors are off.
- On the positive half of the input cycle, once the input signal is greater than 0.7 V, Q1 will turn on and current flows as shown in Fig. Notice that the base-emitter voltage of Q1 causes Q2 to be held in the off state since Q2's base-emitter is reverse biased.
- As the input signal swings into the negative half of its cycle and exceeds 0.7V, Q2 is turned on and its base-emitter voltage reverse biases the base-emitter junction of Q1, turning it off.
- Typical output waveforms for both Q1 and Q2 BJTs and a Class B amplifier output are shown in Fig.
- The time required for the input signal to move from zero volts to +0.7 V or to -0.7 V is the time during which conduction does not occur, consequently the output sits at zero

volts for this interval, producing what is called *crossover distortion*. Crossover distortion takes its name from the dead-time distortion occurring when the input crosses over from -0.7 V to +0.7 V or from +0.7 V to -0.7 V.

- *Class B* has a very low (almost zero) Quiescent Current, and hence low standing power dissipation and optimum power efficiency. However it should be clear that in practice Class B may suffer from problems when handling low-level signals. In the absence of an input signal, a Class B power amplifier should have zero volts dc on the output terminal with respect to ground, if the transistors are well matched. Often, they are not well matched, so the student should be aware that it is quite possible to have a dc voltage present at the output. Some output loads, such as speakers, may be damaged by dc. If such loads are to be used, they must be capacitively coupled to the output in order to block the dc.

Power Amplifier Class AB

Crossover distortion could be eliminated in class AB power amplifiers by the addition of the diode circuitry shown in Fig.



a) Class AB circuit diagram b) Class AB output waveforms

Fig. Class AB power amplifier circuit

Since the diodes in Fig. are on all the time, both Q1 and Q2 are held at the edge of the conduction mode by the diode voltages (A small but controlled Quiescent Current). When the input goes either positive or negative, very little voltage is required to put Q1 or Q2 into full conduction. Typical output waveforms for both Q1 and Q2 BJTs and a Class AB amplifier output are shown in Fig.

$$A_V[dB] = 20\log\left|\frac{V_o}{V_{in}}\right| \qquad \text{.....(1)}$$

$$A_P[dB] = 10\log\left|\frac{P_o}{P_{in}}\right| \qquad \text{.....(2)}$$

$$P_{DC}=V_{DC}I_{DC}=V_{DC}\frac{2}{\pi}I_{op}=V_{DC}\frac{2}{\pi}\frac{V_{OP}}{R_L} \qquad \text{……..(3)}$$

$$P_{OAC}=\frac{V_O{}^{2}{}_{(rms)}}{R_L}=\frac{V_O{}^{2}{}_{(P)}}{2R_L} \qquad \text{……..(4)}$$

$$\eta=\frac{P_{o\,AC}}{P_{DC}} \qquad \text{.....(5)}$$

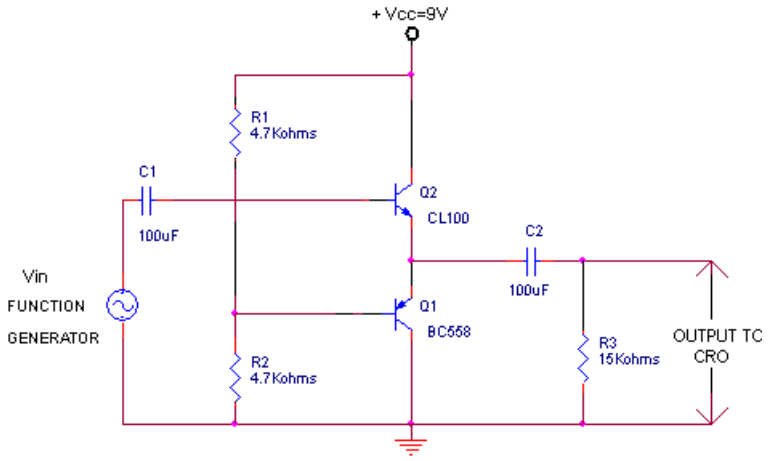
EXPERIMENT -9

Aim:- To study the characteristics symmetry amplifier.

Apparatus:-

1.Transistor CL100, BC558 1,1
2. Resistor 4.7k_,15k_ 2,1
3. Capacitor 100µF 2
4. Diode IN4007 2
5. Signal Generator (0-3)MHz 1
6. CRO 30MHz 1
7. Regulated power supply (0-30)V 1
8. Bread Board 1

Circuit Diagram:-



Formula:

Input power, Pin=2VccIm/П
Output power, Pout=VmIm/2
Power Gain or efficiency, η=л/4(Vm/Vcc) 100

Theory:-

A power amplifier is said to be Class B amplifier if the Q-point and the input signal are selected such that the output signal is obtained only for one half cycle for a full input cycle. The Q-point is selected on the X-axis. Hence, the transistor remains in the active region only for the positive half of the input signal. There are two types of Class B power amplifiers: Push Pull amplifier and complementary symmetry amplifier. In the complementary symmetry amplifier, one n-p-n and another p-np transistor is used. The matched pair of transistor are used in the common collector configuration. In the positive half cycle of the input signal, the n-p-n transistor is driven into active region and starts conducting and in negative half cycle, the p-n-p transistor is driven into conduction. However there is a period between the crossing of the half cycles of the input signals, for which none of the transistor is active and output, is zero.

OBSERVATION

OUTPUT SIGNAL:
AMPLITUDE :
TIME PERIOD :

CALCULATION

POWER, $P_{IN} = 2V_{CC} I_m/л$

OUTPUT POWER, $P_{OUT} = V_m I_m/2$

EFFICIENCY, $\eta = (л/4)(V_m/ V_{CC}) \times 100$

Procedure:-

1. Connections are given as per the circuit diagram without diodes.
2. Observe the waveforms and note the amplitude and time period of the input signal and distorted waveforms.
3. Connections are made with diodes.
4. Observe the waveforms and note the amplitude and time period of the input signal and output signal.
5. Draw the waveforms for the readings.
6. Calculate the maximum output power and efficiency.

Hence the nature of the output signal gets distorted and no longer remains the same as the input. This distortion is called cross-over distortion. Due to this distortion, each transistor conducts for less than half cycle rather than the complete half cycle. To overcomethis distortion, we add 2 diodes to provide a fixed bias and eliminate cross-over distortion.

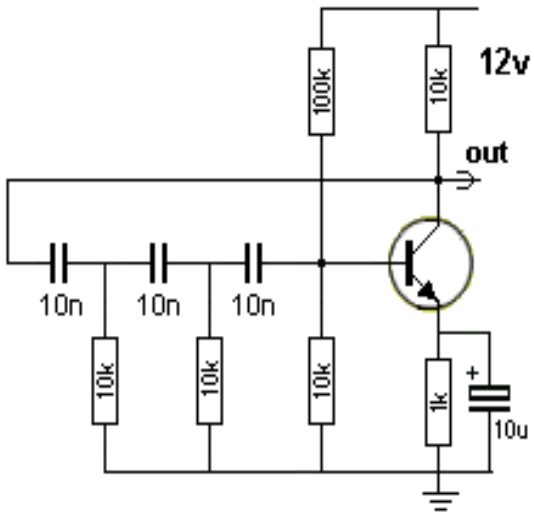
Result:-

EXPERIMENT-10

Aim:- To design and set up an RC phase shift oscillator using BJT and to observe the sinusoidal output waveform.

Apparatus:- Transistor, dc source,capacitors, resistors, potentiometer, breadboard and CRO.

Circuit Diagram:-



Theory:

An oscillator is an electronic circuit for generating an ac signal voltage with a dc supply as the only input requirement. The frequency of the generated signal is decided by the circuit elements. An oscillator requires an amplifier, a frequency selective network, and a positive feedback from the output to the input. The Barkhausen criterion for sustained oscillation is A_ = 1 where A is the gain of the amplifier and is the feedback factor. The unity gain means signal is in phase. (If the signal is 180° out of phase, gain will be 1.). If a common emitter amplifier is used, with a resistive collector load, there is a 180 phase shift between the voltages at the base and the collector. In the figure shown, three sections of phase shift networks are used so that each section introduces approximately 60_ phase shift at resonant frequency. By analysis, resonant frequency f can be expressed by the equation:-

$$f = \frac{1}{2\pi RC\sqrt{6 + 4R_c/R}}$$

Procedure:

1. Connections are made as per circuit diagram.
2. Connect CRO output terminals and observe the waveform.
3. Calculate practically the frequency of oscillations by using the expression f = 1 / T.
4. Repeat the above steps 2,3 for different values of L, and note down the practically values of oscillations
of the RC-phase shift oscillator.

Precautions:-

1. All the connections should be correct.
2. Transistor terminals must be identified properly.
3. Reading should be taken without any parallax error.

Experiment-11

Aim:- Application of Op-Amp(741) as inverting and non-inverting amplifier.

Apparatus:-

1.	Function Generator	3 MHz	1
2.	CRO	30 MHz	1
3.	Dual RPS	0 – 30 V	1
4.	Op-Amp	IC 741	1
5.	Bread Board		1
6.	Resistors	As required	
7.	Connecting wires and probes	As required	

Theory:-

The input signal V_i is applied to the inverting input terminal through R_1 and the non-inverting input terminal of the op-amp is grounded. The output voltage V_o is fed back to the inverting input terminal through the R_f - R_1 network, where R_f is the feedback resistor. The output voltage is given as,

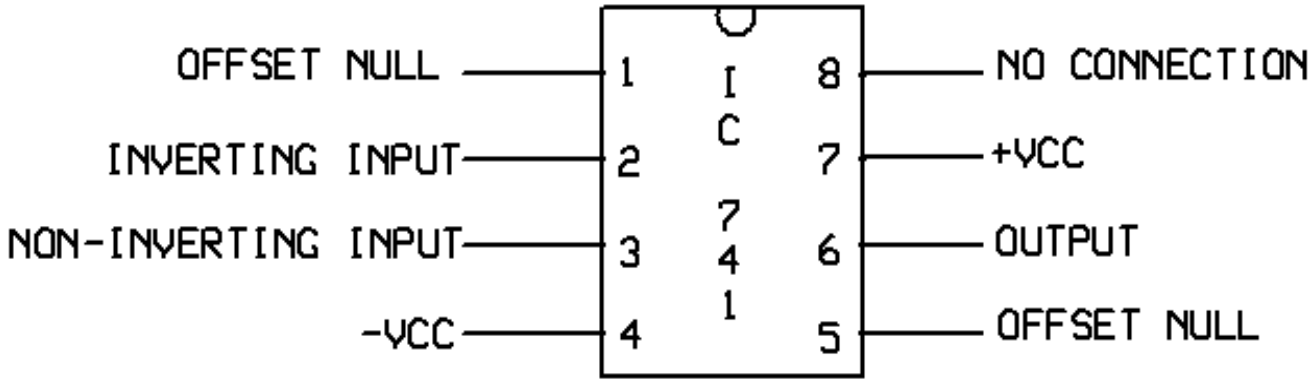
$$V_o = - A_{CL} V_i$$

Here the negative sign indicates that the output voltage is 180^0 out of phase with the input signal.

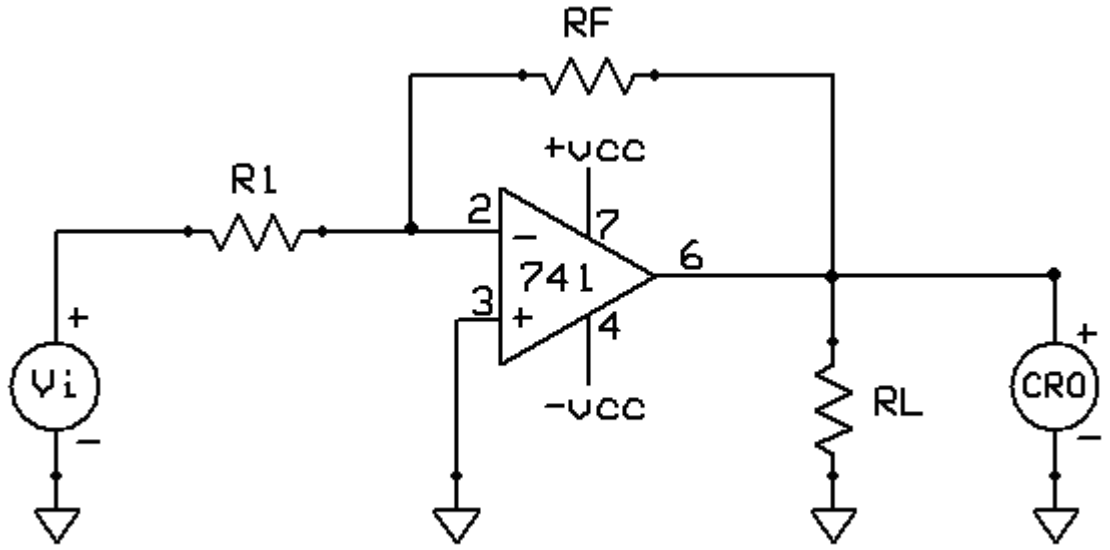
Procedure :-

1. Connections are given as per the circuit diagram.
2. $+ V_{cc}$ and $- V_{cc}$ supply is given to the power supply terminal of the Op-Amp IC.
3. By adjusting the amplitude and frequency knobs of the function generator, appropriate input voltage is applied to the inverting input terminal of the Op-Amp.
4. The output voltage is obtained in the CRO and the input and output voltage waveforms are plotted in a graph sheet.

PIN DIAGRAM:



CIRCUIT DIAGRAM OF INVERTING AMPLIFIER:



DESIGN:

We know for an inverting Amplifier $A_{CL} = R_F / R_1$
Assume R_1 (approx. 10 KΩ) and find R_f
Hence $V_o = - A_{CL} V_i$

OBSERVATIONS:

S.No		Input	Output	
			Practical	Theoretical
1.	Amplitude (No. of div x Volts per div)			
2.	Time period (No. of div x Time per div)			

RESULT:

The design and testing of the inverting amplifier is done and the input and output waveforms were drawn.

Experiment-12

AIM:- NON - INVERTING AMPLIFIER:-

Apparatus:-

S.No	Name of the Apparatus	Range	Quantity
1.	Function Generator	3 MHz	1
2.	CRO	30 MHz	1
3.	Dual RPS	0 – 30 V	1
4.	Op-Amp	IC 741	1
5.	Bread Board		1
6.	Resistors	As required	
7.	Connecting wires and probes	As required	

THEORY:

The input signal V_i is applied to the non - inverting input terminal of the op-amp. This circuit amplifies the signal without inverting the input signal. It is also called negative feedback system since the output is feedback to the inverting input terminals. The differential voltage V_d at the inverting input terminal of the op-amp is zero ideally and the output voltage is given as,

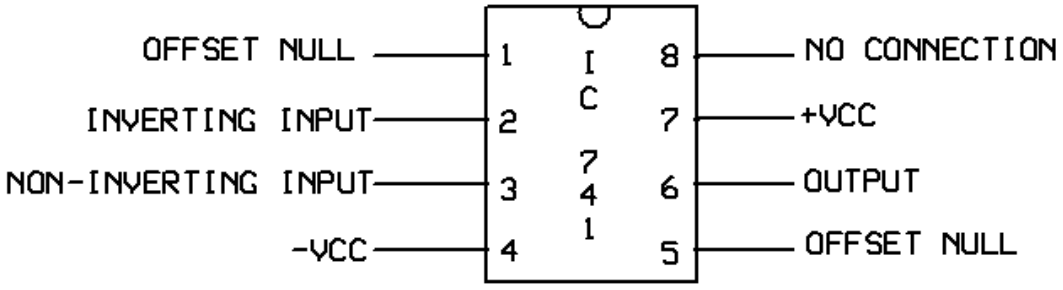
$$V_o = A_{CL} V_i$$

Here the output voltage is in phase with the input signal.

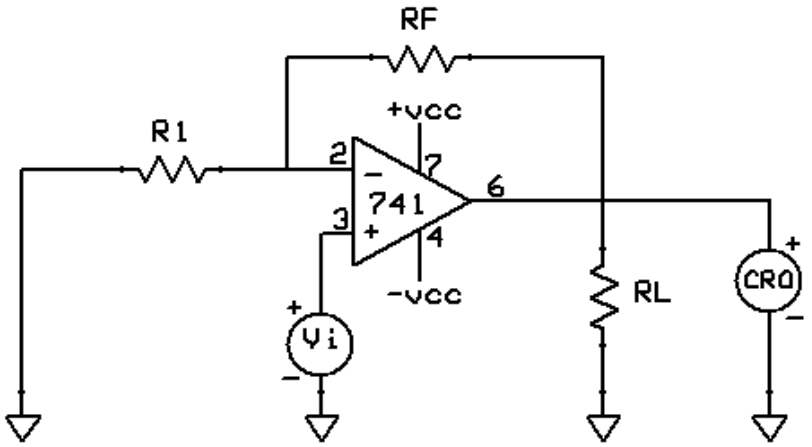
PROCEDURE:

1. Connections are given as per the circuit diagram.
2. $+V_{cc}$ and $-V_{cc}$ supply is given to the power supply terminal of the Op-Amp IC.
3. By adjusting the amplitude and frequency knobs of the function generator, appropriate input voltage is applied to the non - inverting input terminal of the Op-Amp.
4. The output voltage is obtained in the CRO and the input and output voltage waveforms are plotted in a graph sheet.

PIN DIAGRAM:



CIRCUIT DIAGRAM OF NON INVERITNG AMPLIFIER:



DESIGN:

We know for a Non-inverting Amplifier $A_{CL} = 1 + (R_F / R_1)$
Assume R_1 (approx. 10 KΩ) and find R_f
Hence $V_o = A_{CL} V_i$

OBSERVATIONS:

S.No		Input	Output	
			Practical	Theoretical
1.	Amplitude (No. of div x Volts per div)			
2.	Time period (No. of div x Time per div)			

RESULT:

The design and testing of the Non-inverting amplifier is done and the input and output waveforms were drawn.

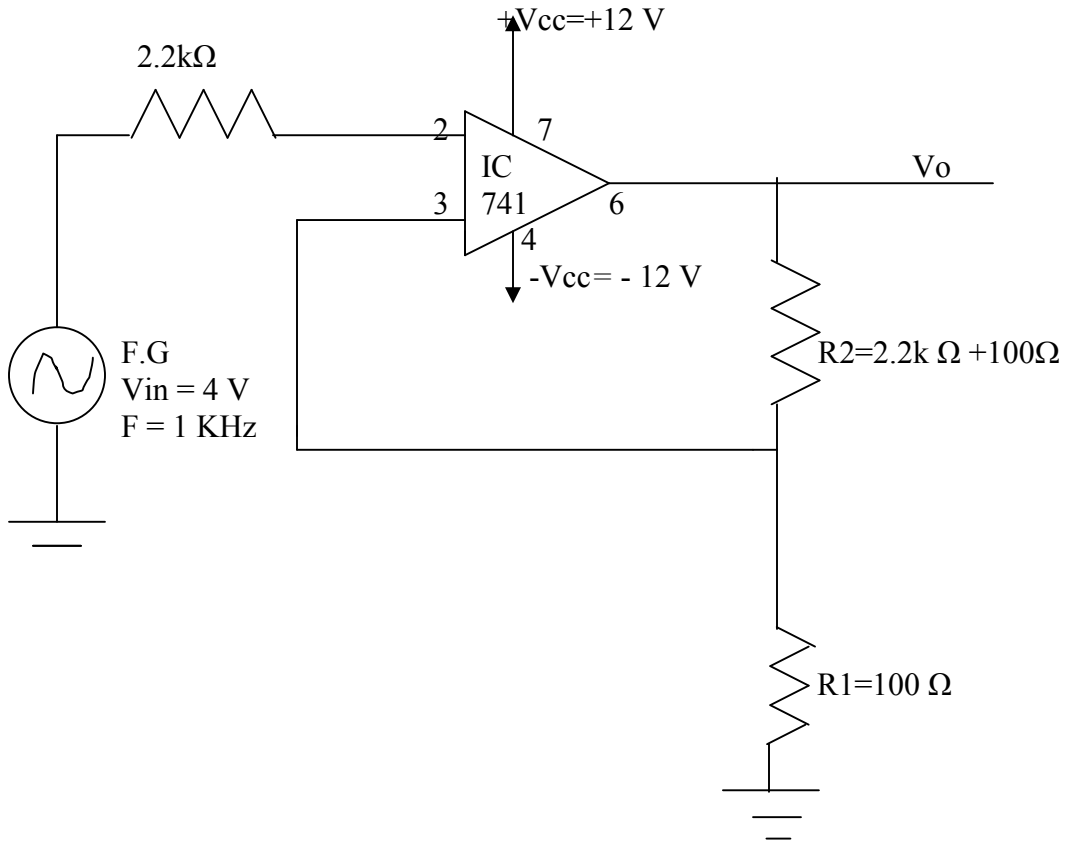
Experiment-13

Aim:- Application of OP-AMP as Schmitt Trigger.

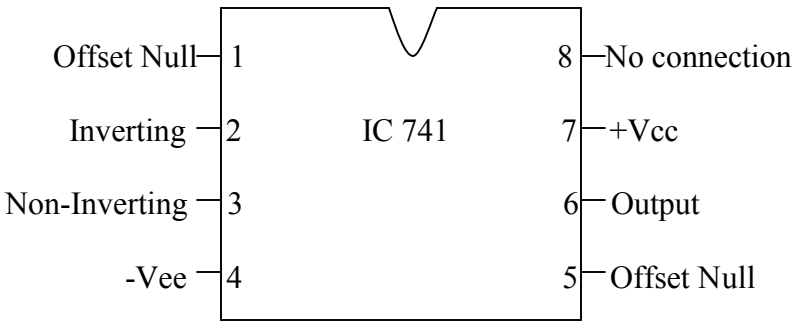
Apparatus:-

S.NO	ITEM	RANGE	Q.TY
1	OP-AMP	IC741	1
2	RESISTOR	100KΩ, 2.2KΩ	2 1
3	CRO	-	1
4	RPS	DUAL(0-30) V	1

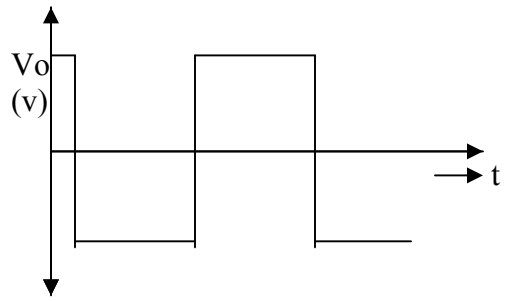
CIRCUIT DIAGRAM:-



Pin Diagram:



O/P wave form:



THEORY:

Schmitt trigger is useful in squaring of slowly varying i/p waveforms.Vin is applied to inverting terminal of op-amp .Feedback voltage is applied to the non-inverting terminal. LTP is the point at which output changes from high level to low level .This is highly useful in triangular waveform generation, wave shape pulse generator, A/D convertor etc.

PROCEDURE :

The connections are made as shown in the circuit diagram.The signal which has to be made square is applied to the inverting terminal . Here the i/p is a sine waveform.The supply voltage is switched ON and the o/p waveform is recorded through CRO.The UTP and LTP are also found and the theoretical and practical values are verified.

$$LTP = R1/(R1 + R2)^{X(-Vsat)}$$
$$UTP = R2/(R1 + R2)^{X(+Vsat)}$$

Design :

+Vsat= +Vcc=15v
-Vsat= -Vee= -15v

RESULT:

The Schmitt trigger circuit is connected and the waveforms are drawn and theoretical and practical values for the trip points are verified.

Theoretical values =
Practical values =

EXPERIMENT-14

Aim :- **Design the monostable multivibrator using the IC555.**

Apparatus :-

S.NO	ITEM	RANGE	Q.TY
1	IC	NE555	1
2	RESISTOR	9KΩ	1
3	CAPACITOR	0.01μF 0.1μF	1 1
4	RPS	(0-30) V	1
5	CRO	-	1

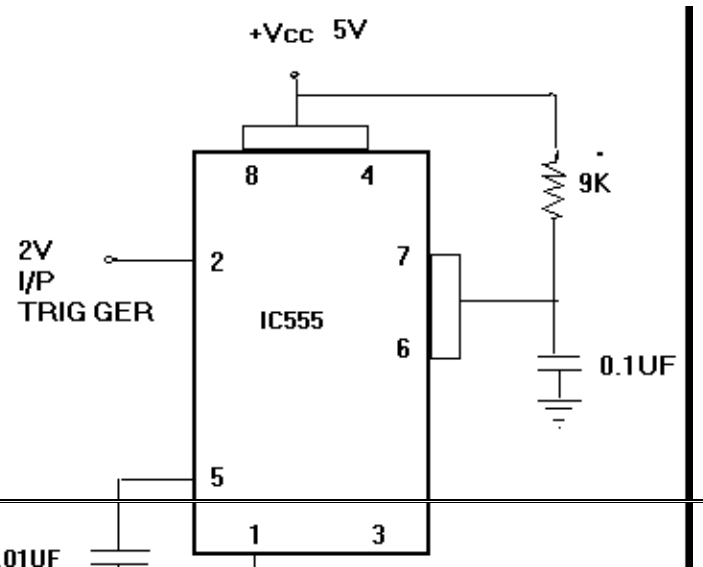
THEORY:

A monostable multivibrator has one stable state and a quasistable state. When it is triggered by an external agency it switches from the stable state to quasistable state and returns back to stable state. The time during which it states in quasistable state is determined from the time constant RC. When it is triggered by a continuous pulse it generates a square wave. Monostable multi vibrator can be realized by a pair of regeneratively coupled active devices, resistance devices and op-amps.

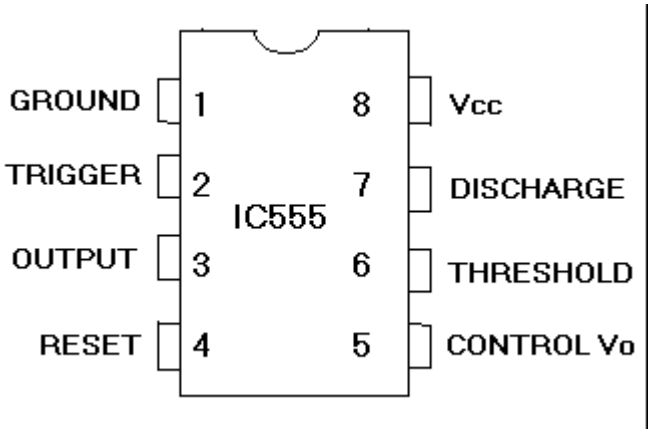
DESIGN :

$T = 0.1ms$
$C = 0.01\mu F$
$T = 1.096RC$
$R = T / 1.096C = (0.1*10^{-3}) / (1.096*0.01*10^{-6})$
$= 9.12\ K\Omega$
$R \cong 9\ K\Omega$

Circuit Diagram



PIN DIAGRAM:-



PROCEDURE:

The connections are made as per the diagram. The value of R is chosen as 9kΩ. The DCB is set to the designed value. The power supply is switched on and set to +5V. The output of the pulse generator is set to the desired frequency. Here the frequency of triggering should be greater than width of ON period (i.e.) T >W. The output is observed using CRO and the result is compared with the theoretical value. The experiment can be repeated for different values of C and the results are tabulated.

OBSERVATION:-

C (uf)	Theoritical(T=1.095 RC(ms)))	Practical T(ms)

RESULT:

Thus the monostable multivibrator using IC555 is designed and its output waveform is traced

`EXPERIMENT-15 **APPLICATION OF IC555 AS AN ASTABLE MULTIVIBRATOR.**

Aim: To study the application of IC555 as an Astable multivibrator.

Apparatus:-

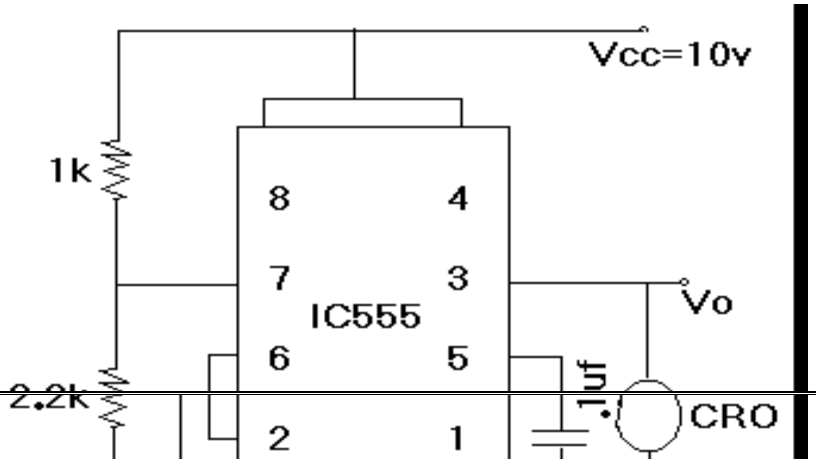
S.NO	ITEM	RANGE	Q.TY
1	IC	NE555	1
2	RESISTOR	1KΩ, 2.2KΩ	1 1
3	CAPACITOR	0.1μF 0.01μF	1 1
4	CRO	-	1
5	RPS	DUAL(0-30) V	1

Theory:

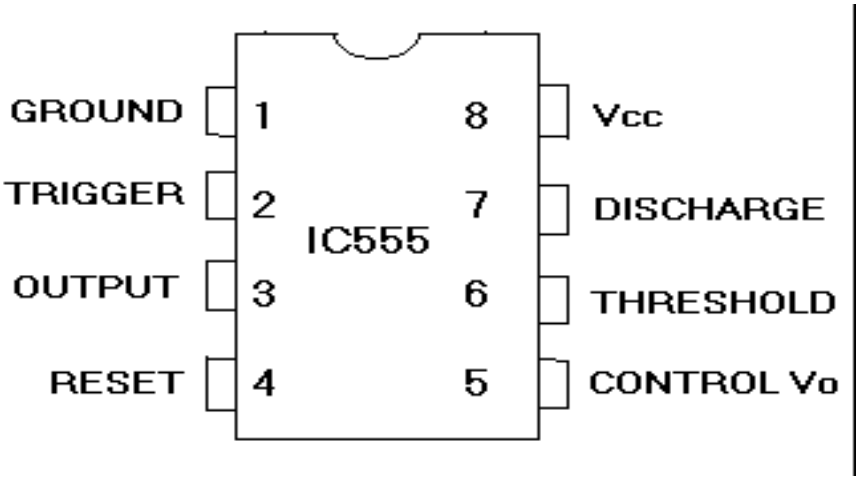
The IC555 timer is a 8 pin IC that can be connected to external components for astable operation. The simplified block diagram is drawn. The OP-AMP has threshold and control inputs. Whenever the threshold voltage exceeds the control voltage, the high output from the OP –AMP will set the flip-flop. The collector of discharge transistor goes to pin 7. When this pin is connected to an external trimming capacitor, a high Q output from the flip flop will saturate the transistor and discharge the capacitor. When Q is low the transistor opens and the capacitor charges.

The complementary signal out of the flip-flop goes to pin 3 and output. When external reset pin is grounded it inhibits the device. The on – off feature is useful in many application. The lower OP- AMP inverting terminal input is called the trigger because of the voltage divider. The non-inverting input has a voltage of +Vcc/3, the OP-Amp output goes high and resets the flip flop.

Circuit diagram:



PIN DIAGRAM:-



Procedure :

The connections are made as per the circuit diagram and the values of R and C are calculated assuming anyone term and they are settled . The output waveform is noted down and graph is drawn and also the theoretical and practical time period is verified.

Observation:

C (uf)	Theoretical time period(us)	Practical time period(us)	Theoretical freq (kHz)	Practical freq(kHz)

Calculation:

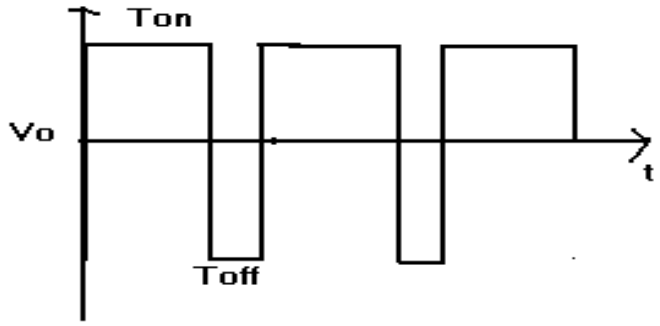
Theoretical:

$T = 0.69(Ra+Rb)C=0.69(1*10^3 + 2.2*10^3)*0.01*10^{-6}) = 0.22\mu s$

Practical:

T = Ton + Toff

MODEL GRAPH:



Result :

Thus the astable multivibrator circuit using IC555 is constructed and verified its theoretical and practical time period.

EXPERIMENT-16

Aim:- **To study the operation of Arithmetic Logic Unit IC 74181.**

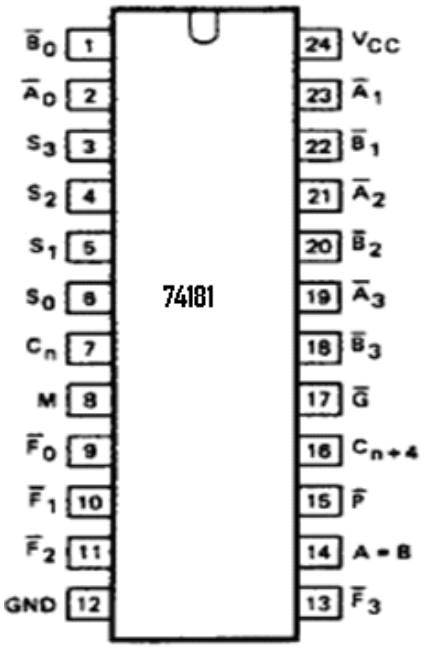
Apparatus:- IC 74181, etc.

Pin detail & Function table:-

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 22, 20, 18	$\overline{B}_0$ to $\overline{B}_3$	operand inputs (active LOW)
2, 23, 21, 19	$\overline{A}_0$ to $\overline{A}_3$	operand inputs (active LOW)
6, 5, 4, 3	S_0 to S_3	select inputs
7	C_n	carry input
8	M	mode control input
9, 10, 11, 13	$\overline{F}_0$ to $\overline{F}_3$	function outputs (active LOW)
12	GND	ground (0 V)
14	A=B	comparator output
15	$\overline{P}$	carry propagate output (active LOW)
16	C_{n+4}	carry output
17	$\overline{G}$	carry generate output (active LOW)
24	V_{CC}	positive supply voltage

Pin Detail :-


$\overline{B}_0$ 1
$\overline{A}_0$ 2
S_3 3
S_2 4
S_1 5
S_0 6
C_n 7
M 8
$\overline{F}_0$ 9
$\overline{F}_1$ 10
$\overline{F}_2$ 11
GND 12
74181
24 V_{CC}
23 $\overline{A}_1$
22 $\overline{B}_1$
21 $\overline{A}_2$
20 $\overline{B}_2$
19 $\overline{A}_3$
18 $\overline{B}_3$
17 $\overline{G}$
16 C_{n+4}
15 $\overline{P}$
14 A = B
13 $\overline{F}_3$

FUNCTION TABLES

MODE SELECT INPUTS				ACTIVE HIGH INPUTS AND OUTPUTS	
S_3	S_2	S_1	S_0	LOGIC (M=H)	ARITHMETIC(2) (M=L; C_n=H)
L	L	L	L	$\overline{A}$	A
L	L	L	H	$\overline{A+B}$	A + B
L	L	H	L	$\overline{A}B$	$A+\overline{B}$
L	L	H	H	logical 0	minus 1
L	H	L	L	$\overline{AB}$	A plus $A\overline{B}$
L	H	L	H	$\overline{B}$	(A + B) plus $A\overline{B}$
L	H	H	L	$A \oplus B$	A minus B minus 1
L	H	H	H	$A\overline{B}$	$A\overline{B}$ minus 1
H	L	L	L	$\overline{A}+B$	A plus AB
H	L	L	H	$\overline{A \oplus B}$	A plus B
H	L	H	L	B	$(A+\overline{B})$ plus AB
H	L	H	H	AB	AB minus 1
H	H	L	L	logical 1	A plus A(1)
H	H	L	H	$A+\overline{B}$	(A + B) plus A
H	H	H	L	A + B	$(A+\overline{B})$ plus A
H	H	H	H	A	A minus 1

Notes to the function tables

1. Each bit is shifted to the next more significant position.
2. Arithmetic operations expressed in 2s complement notation.

H = HIGH voltage level
L = LOW voltage level

MODE SELECT INPUTS				ACTIVE LOW INPUTS AND OUTPUTS	
S_3	S_2	S_1	S_0	LOGIC (M=H)	ARITHMETIC(2) (M=L; C_n=L)
L	L	L	L	$\overline{A}$	A minus 1
L	L	L	H	$\overline{AB}$	AB minus 1
L	L	H	L	$\overline{A}+B$	$A\overline{B}$ minus 1
L	L	H	H	logical 1	minus 1
L	H	L	L	$\overline{A+B}$	A plus $(A+\overline{B})$
L	H	L	H	$\overline{B}$	AB plus $(A+\overline{B})$
L	H	H	L	$\overline{A \oplus B}$	A minus B minus 1
L	H	H	H	$A+\overline{B}$	$A+\overline{B}$
H	L	L	L	$\overline{AB}$	A plus (A + B)
H	L	L	H	$A \oplus B$	A plus B
H	L	H	L	B	$A\overline{B}$ plus (A + B)
H	L	H	H	A + B	A + B
H	H	L	L	logical 0	A plus A(1)
H	H	L	H	$A\overline{B}$	AB plus A
H	H	H	L	AB	$A\overline{B}$ plus A
H	H	H	H	A	A

Notes to the function tables

1. Each bit is shifted to the next more significant position.
2. Arithmetic operations expressed in 2s complement notation.

H = HIGH voltage level
L = LOW voltage level

AIM: To study about logic gates and verify their truth tables.

APPARATUS REQUIRED:

SL No.	COMPONENT	SPECIFICATION	QTY
1.	AND GATE	IC 7408	1
2.	OR GATE	IC 7432	1
3.	NOT GATE	IC 7404	1
4.	NAND GATE 2 I/P	IC 7400	1
5.	NOR GATE	IC 7402	1
6.	X-OR GATE	IC 7486	1
7.	NAND GATE 3 I/P	IC 7410	1
8.	IC TRAINER KIT	-	1
9.	PATCH CORD	-	14

THEORY:

Circuit that takes the logical decision and the process are called logic gates. Each gate has one or more input and only one output.

OR, AND and NOT are basic gates. NAND, NOR and X-OR are known as universal gates. Basic gates form these gates.

AND GATE:

The AND gate performs a logical multiplication commonly known as AND function. The output is high when both the inputs are high. The output is low level when any one of the inputs is low.

OR GATE:

THE OR GATE PERFORMS A LOGICAL ADDITION COMMONLY KNOWN AS OR FUNCTION. THE OUTPUT IS HIGH WHEN ANY ONE OF THE INPUTS IS HIGH. THE OUTPUT IS LOW LEVEL WHEN BOTH THE INPUTS ARE LOW.

NOT GATE:

The NOT gate is called an inverter. The output is high when the input is low. The output is low when the input is high.

NAND GATE:

The NAND gate is a contraction of AND-NOT. The output is high when both inputs are low and any one of the input is low .The output is low level when both inputs are high.

NOR GATE:

The NOR gate is a contraction of OR-NOT. The output is high when both inputs are low. The output is low when one or both inputs are high.

X-OR GATE:

The output is high when any one of the inputs is high. The output is low when both the inputs are low and both the inputs are high.

PROCEDURE:

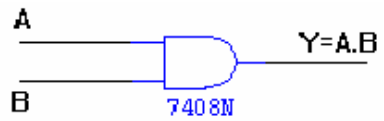
(i) Connections are given as per circuit diagram.

(ii) Logical inputs are given as per circuit diagram.

(iii) Observe the output and verify the truth table.

AND GATE:

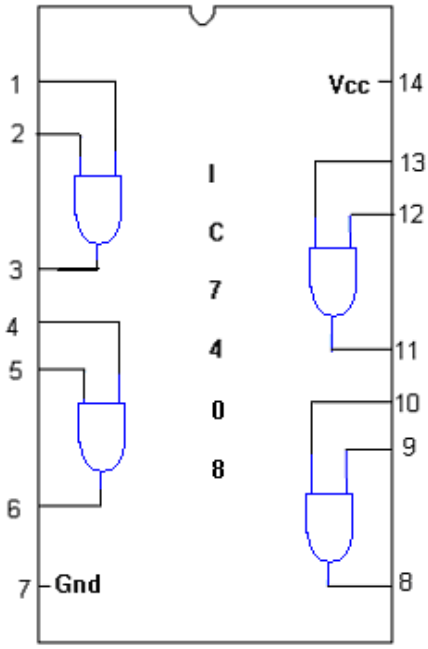
SYMBOL:



TRUTH TABLE

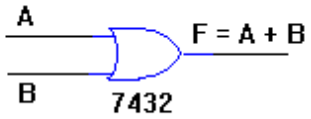
A	B	A.B
0	0	0
0	1	0
1	0	0
1	1	1

PIN DIAGRAM:

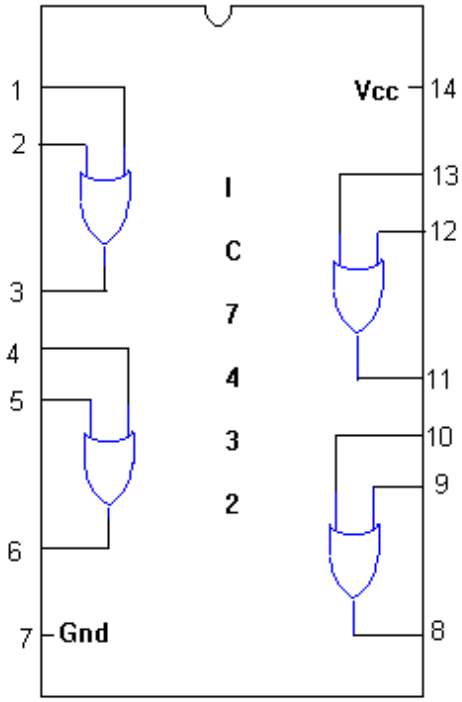


OR GATE:

SYMBOL :



PIN DIAGRAM :



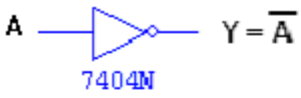
TRUTH TABLE

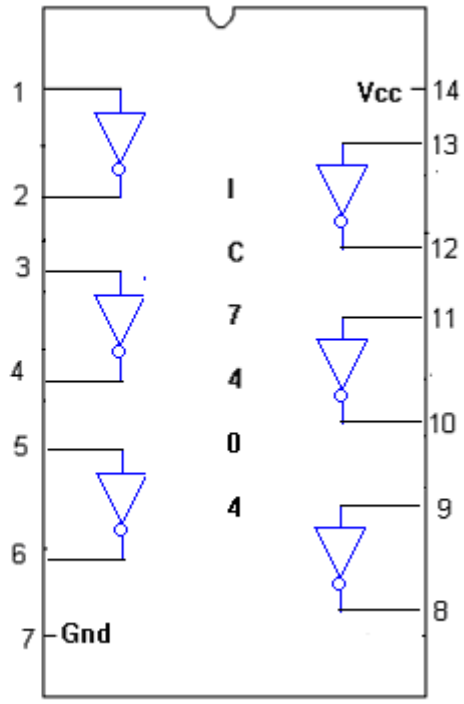
A	B	A+B
0	0	0
0	1	1
1	0	1
1	1	1

NOT GATE:

SYMBOL:

PIN DIAGRAM:



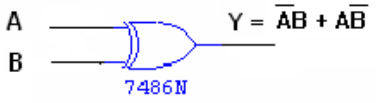


TRUTH TABLE :

A	$\overline{A}$
0	1
1	0

X-OR GATE :

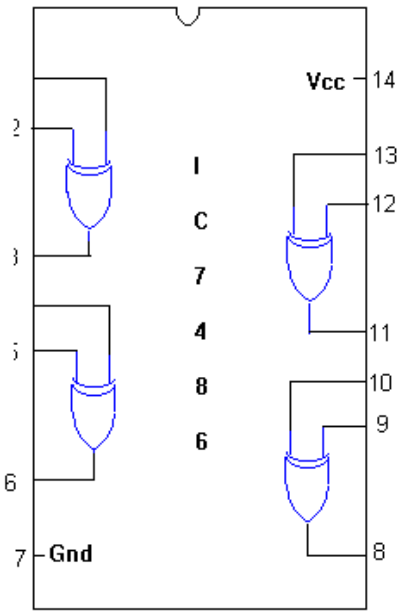
SYMBOL :



TRUTH TABLE :

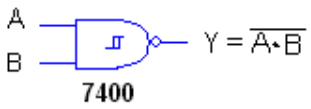
A	B	$\overline{A}B + A\overline{B}$
0	0	0
0	1	1
1	0	1
1	1	0

PIN DIAGRAM :



2-INPUT NAND GATE:

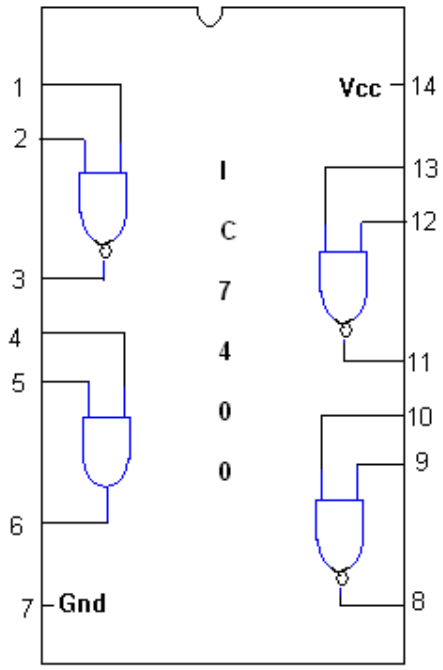
SYMBOL:



TRUTH TABLE

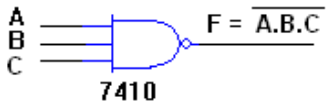
A	B	$\overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

PIN DIAGRAM:

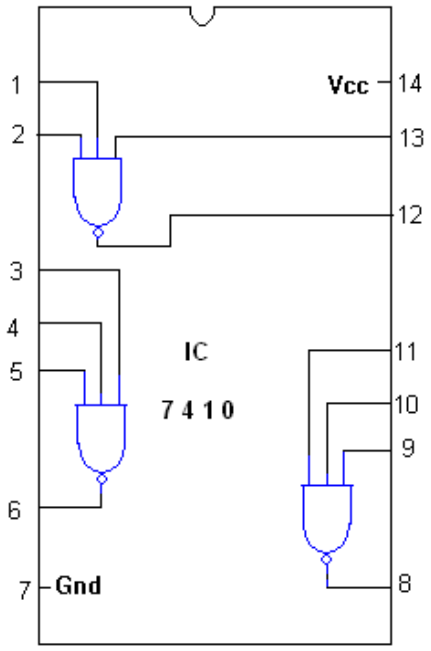


3-INPUT NAND GATE :

SYMBOL :



PIN DIAGRAM :

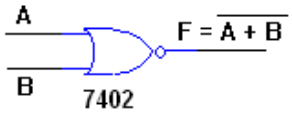


TRUTH TABLE

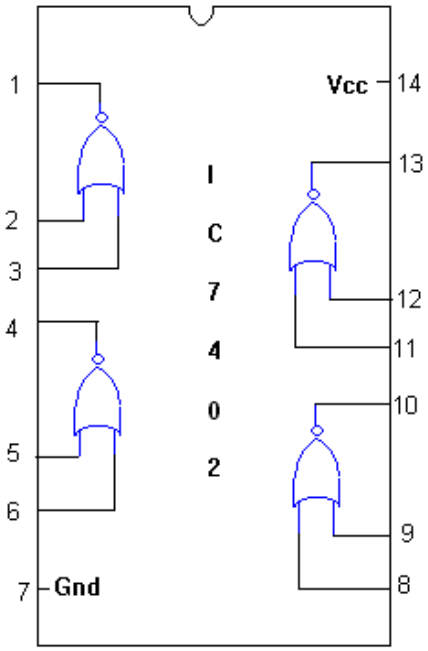
A	B	C	$\overline{A.B.C}$
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

NOR GATE:

SYMBOL :



PIN DIAGRAM :



TRUTH TABLE

A	B	$\overline{A+B}$
0	0	1
0	1	1
1	0	1
1	1	0